MODEL 275B

T3 TRANSMISSION TEST SET

OPERATING MANUAL

Bowmar

WHEN QUALITY COUNTS

Communication Test Equipment

Bowmar/ALI Inc.
531 Main Street
Acton, Mass. 01720

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MANUFACTURED BY:

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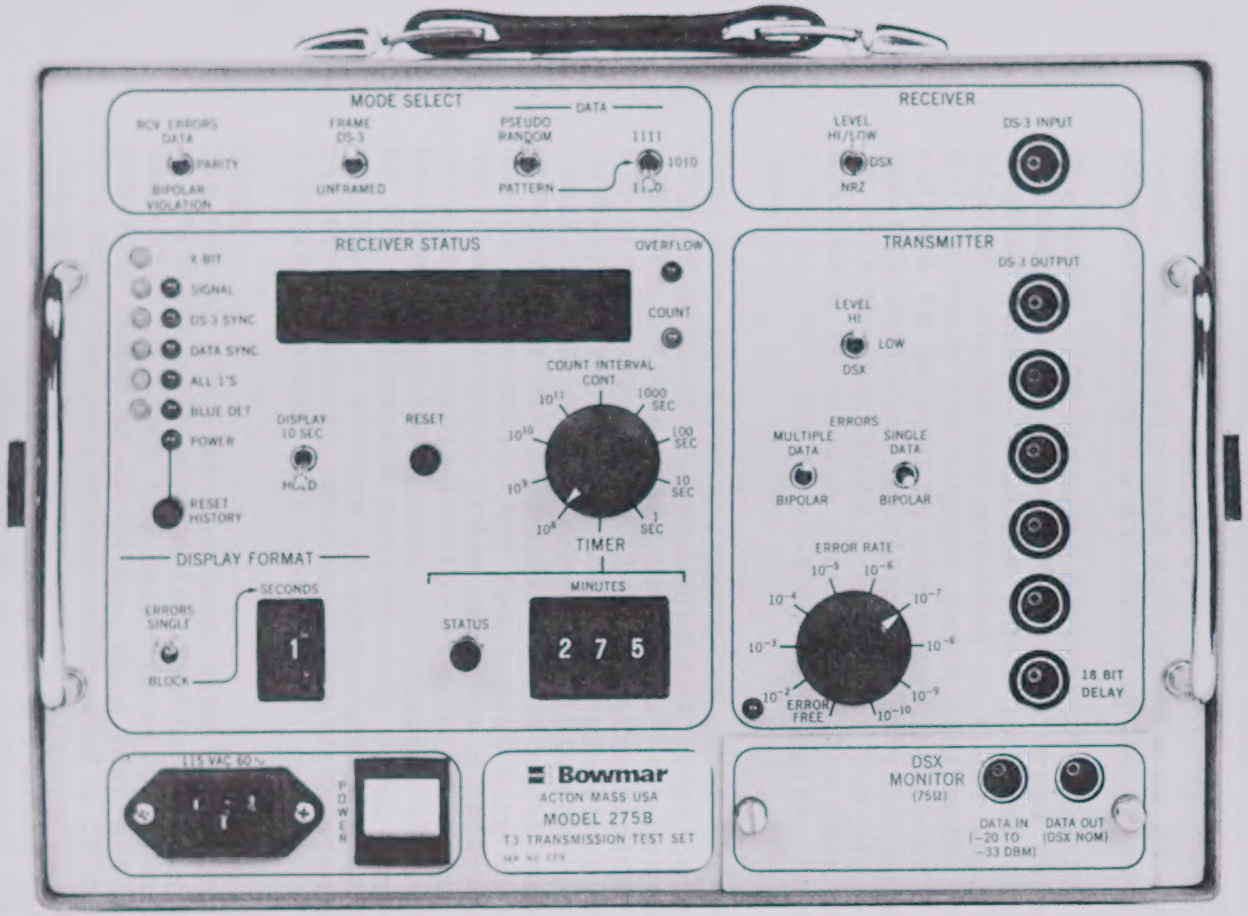



MODEL 275B

T3 TRANSMISSION TEST SET

## 1.0 GENERAL

The Bowmar Model 275B Transmission Test Set is a rugged field instrument incorporating both transmitter and receiver within one case measuring less than one cubic foot. A small package with a wide range of features for test, installation and maintenance of T3 system components in radio and fiber optic transmission systems.

The Model 275B connects directly to the T3 system at standard Low, Hi and DSX3 system cross connects and monitor jacks. A single input jack and six independent bipolar outputs are provided to fully load M34 multiplexers and digital radio equipment. One of the six outputs is delayed by eighteen time slots. A -20 to -33 dBm DSX amplifier provides the additional gain to operate at DSX3 monitor jacks. Either of two plug-in modules available as options provide NRZ I/O data and clock at $\pm$ 1 volt., 75 ohms or -0.9 to -1.8 volts, 50 ohm signal levels.

Four data patterns are provided which are transmitted with or without the standard DS3 frame format. The data patterns include a 32,767 bit ($2^{15}$-1) pseudorandom word, all ones, alternating 1100 and alternating 1010 (blue pattern). The pseudorandom pattern simulates live traffic loading on a communications channel. Unframed pseudorandom data, because of its short resync time, is useful in investigating radio switching time. The all one's data without frame provides a reference signal for calculating signal levels. The blue signal provides testing of system alarms. Comparing the bit error rate of the pseudorandom pattern with other patterns establishes a measure of system pattern sensitivity. All patterns produced are compatible with system generated signals or other test equipment.

### 1.1 Scope

The manual provides the user with both operation and calibration/maintenance information. This manual is dedicated to teach the basic function of all controls and provides examples as to how this test set may be used to determine the performance status of a T3 carrier communication system or system component. As this test set was designed to operate with a broad category of equipment manufactured by many different companies, it is difficult to provide specific information. The user should be familiar with the equipment to be tested and

test procedures specifically developed for that particular system.

## 1.2 Specification Summary

**SPECIFICATIONS**

**BIPOLAR OUTPUTS** Six independent, B3ZS coded, unbalanced, 75 ohm outputs, at three switch selectable levels. Three jack styles are available: WECO 440 (Standard), WECO 358 (Option), BNC (Option).

**High Level:** 0.91V peak ± 1.2 dB, 4.5 ± 1.5 nsec rise-fall time (7.4 dBm nominal)

**DSX Level:** High output passed through a 450 foot 728A cable simulator.

**Low Level:** High output flat attenuated by 13.8 dB, 0.186V peak ± 2.0 dB (-6.4 dBm nominal)

**Delay:** 18 time slot delayed output is provided as one of the six standard outputs.

**BINARY OUTPUTS/INPUTS**
Optional, XMT/RCV NRZ data and clock at ± 1.0V peak amplitude on 75 ohm unbalanced BNC connectors. Receiver sensitivity to 250 mV peak (Plug-in Module 2753-1).

Optional, XMT/RCV NRZ data and clock at -0.9 to -1.8 volts on 50 ohm, unbalanced BNC connectors (Plug-in Module 2753-2).

**DATA RATE**
44.736 MHz ± 20 PPM, 0 to 50°C, 115V ± 10%.

**ERROR INSERTION**
Data or bipolar errors are inserted by the transmitter at a switch selectable rate of $10^{-N}$ for N = 2, 3, 4, 5, 6, 7, 8, 9, 10, error free and single. Data errors are inserted after parity calculation and will produce parity errors provided the error rate does not result in an even number of errors in one frame.

**BIPOLAR INPUT**
One B3ZS coded, 75 ohm unbalanced input; switch selectable input for standard Low, High and DSX levels.

**MONITOR AMPLIFIER INPUT**
Standard, compatible with DSX3 inputs from monitor jacks at -20 to -33 dBm.

**ERROR DETECTION**

| | |
|---|---|
| **Data Error:** | Received data is compared with internal pseudorandom data generator ($2^{15}$-1), all 1's, alternating 1100 or alternating 1010 data in either framed or unframed format. |
| **Parity Error:** | Parity is calculated on received data and compared with the frame code parity bits. Any framed data pattern including live traffic is acceptable. |
| **Bipolar Violation:** | Bipolar errors are detected as two consecutive pulses of the same polarity which do not conform to the B3ZS zero substitution code. |
| **Count Interval:** | $10^{8}$ thru $10^{11}$ bit times, 1 Sec. thru 1000 Sec. plus timed and overflow. |

Errors may be counted individually or formatted into asynchronous or synchronous blocks of one (error second) to nine seconds in one-second steps.

**TIMER**
Range of 1 to 999 minutes in one minute steps. Test time to completion may be displayed.

**DISPLAY**
Switch selectable display modes provide a 10 second hold before restarting test or indefinite hold until manually reset.

**PRINTER INTERFACE**
Serial RS232C ASCII data format at 300 Baud (110 Baud Optional) - Selectable NORMAL/INVERTED Printing Mode.

**DATA PATTERNS**
Four switch selectable patterns transmitted with or without standard DS3 frame code.
Patterns: Pseudorandom ($2^{15}$-1)
All 1's
Alternating 1100
Alternating 1010 (blue pattern if framed)

**STATUS INDICATORS**
X-Bit detect, Signal Loss plus History, DS3 Sync plus History, Data Sync plus History, All 1's Detect plus History, Blue Pattern Detect plus History and Power Loss. History indicators are resettable without interfering with test in progress or by manual test reset.

**REAR PANEL**
Transmit and receive word sync on ECL compatible 50 ohms unbalanced BNC connectors. One output pulse is generated for every 32,767 bit pseudorandom word (approximately 22.3 nsec width).

Transmit and receive M-Bit sync on TTL compatible BNC connectors. One pulse coincident with M1 bit in frame code (approximately 2 usec width).

Transmit X-Bit switch forces X-Bits in transmitted frame to ones.

External clock (ECL - 75 ohm compatible)

**INPUT/OUTPUT JACKS**
AT&T Technology 440 equivalent jacks are standard for both 275B and its monitor amplifier. AT&T Technology 358 equivalent or industry standard BNC jacks are available on special order.

**PRIMARY POWER**
115V $\pm$ 10%, 47 to 63 Hz single phase approximately 75 watts.

**OPERATING ENVIRONMENT**
$0^{o}$ to $50^{o}$C ($32^{o}$ to $120^{o}$F) to 95% relative humidity non-condensing.

**SIZE**
8 1/4" H x 11 1/2" W x 12" D

**WEIGHT**
20 lbs nominal

## 2.0 INSTALLATION AND SELF TEST

### 2.1 Preparation

Remove the Model 275B, T3 Transmission Test Set, from its shipping container. Remove the front cover and unwrap the power cord. Connect the Test Set to a standard 115V AC, 50 - 60 Hz, single phase power source. Set the POWER switch to ON and note that this self illuminated switch and any combination of display LEDs are lit. If none of these indicators are lit, turn the power OFF and check for a good 3 AG, 2A slow-blow fuse (rear panel). It is recommended that the self test procedure be completed next to both familiarize the operator with the Test Set's controls and identify any performance problems which may have resulted from shipping. This equipment has been operated for minimum of 100 hours and re-calibrated before shipping to insure product quality.

### 2.2 Self Test Procedure

The following paragraphs provide a procedure for testing the full capability of the Test Set. To proceed, connect the one foot cable provided between the DS-3 INPUT jack and the first (top) DS-3 OUTPUT jack. This procedure loops the Test Set's transmitter section back to its own receiver.

2.2.1 Set these switches to the following initial positions:

| | |
|---|---|
| OUTPUT | - to DISPLAY |
| ERROR FORMAT | - to DATA |
| FRAME | - to DS3 |
| DATA | - to PATTERN and 1111 (ALL 1's) |
| RECEIVER LEVEL | - to HI/LOW |
| TRANSMIT LEVEL | - to HI |
| ERROR RATE | - to ERROR FREE |
| DISPLAY | - to 10 SEC |
| COUNT INTERVAL | - to $10^8$ |
| RESET | - to Momentarily Actuate & Release |

2.2.2 Observe indicators for the following initial response:

| | |
|---|---|
| X-BIT | - Off |
| SIGNAL | - Both Off |
| DS3 SYNC | - Both Off |
| DATA SYNC | - Both Off |
| ALL 1's | - Yellow On - Red Off |
| BLUE DET | - Off |
| POWER | - Off |
| OVERFLOW | - Off |
| COUNT | - On for approximately 2 Sec. and Off for 10 Sec. continually repeating sequence. |

2.2.3 **Transmitter Outputs -**
Remove the plug from the first transmitter output and insert it into the next one down. Observe that the yellow SIGNAL and DATA SYNC indicators are lit when the loop is broken and off as soon as the plug is re-inserted. Disregard all other indicators at this time. Repeat this procedure for the next four DS-3 OUTPUTS.

2.2.4 **Receiver/Transmitter Level -**
Set the DISPLAY switch to HOLD. With the RECEIVE LEVEL switch set to HI/LOW move the Transmit Level switch to LOW. Momentarily push the RESET switch. All indicators should be off except ALL 1's yellow and COUNT. Set both the Receive and Transmit LEVEL switches to DSX. Operate the RESET switch and observe all indicators are off except ALL 1's yellow (continuously ON) and COUNT (ON for approximately 2 Sec.). No errors should accumulate on the display.

To test the NRZ option (if provided) connect one cable between RCV DATA and XMT DATA with another cable between RCV CLOCK and XMT CLOCK. These connectors are located on the NRZ module. Set the Receive Level switch to NRZ and operate the RESET switch. All indicators should be off except ALL 1's and COUNT.

**Test Monitor Module** (27 dB Flat Loss Attenuator 75 ohm) -
Return the Receive and Transmit LEVEL switches to their HI/LOW and HI positions respectively.

2.2.5 **DATA -**
Set the DATA switches to PATTERN and 1111. Operate the RESET switch and observe that all indicators are off except ALL 1's yellow and COUNT. Move the DATA switch from 1111 to 1010. Note that ALL 1's yellow is replaced by its red history indicator. Operate the RESET switch. All indicators should be off except X-BIT, BLUE DET (yellow) and COUNT. Set the DATA switch to 1100 and note

that the BLUE DET yellow indicator is replaced by BLUE DET red. Operate the RESET switch and observe that all indicators are off except COUNT. Locate the X-BIT indicator on the Test Set's rear panel. When pushed, the X-BIT indicator on the front panel should light. Set the DATA switch to PSEUDORANDOM and press RESET. All indicators should be off except COUNT. Remove the plug from the DS-3 INPUT and push the RESET switch. The SIGNAL, DS-3 SYNC and DATA SYNC indicators (yellow) should be lit. Re-insert the plug into the receive DS-3 INPUT. The three yellow indicators should be replaced by their red, history, counterparts. Disregard the status of all other indicators. Set the FRAME switch to UNFRAMED and operate the RESET switch. The yellow DS-3 SYNC indicator should be lit.

2.2.6 **Errors - Display Mode**

Set these switches to the following initial conditions:

| | |
|---|---|
| OUTPUT | - to DISPLAY |
| FRAME | - to DS-3 |
| RCV ERRORS | - to DATA |
| COUNT INTERVAL | - to $10^8$ |
| DISPLAY | - to 10 SEC |
| DISPLAY FORMAT, ERRORS | - to SINGLE |
| Transmitter, ERROR MULTIPLE | - to DATA |
| ERROR RATE | - to $10^{-7}$ |

Momentarily depress RESET

The COUNT indicator should be lit for two seconds and off ten seconds, approximately. While lit the display should count from zero to ten. The following chart lists combinations of switch positions for the COUNT INTERVAL and ERROR RATE switches with the expected displayed result.

Complete all entries:

| COUNT INTERVAL | ERROR RATE | DISPLAYED RESULT | REQUIRED TEST TIME |
|---|---|---|---|
| 1 SEC. | $10^{-2}$ | 450000 ± 1% | 1 SEC. |
| 1 SEC. | $10^{-3}$ | 45000 ± 1% | 1 SEC. |
| 10 SEC. | $10^{-4}$ | 45000 ± 1% | 10 SEC. |
| 100 SEC. | $10^{-5}$ | 45000 ± 1% | 100 SEC. |
| 1000 SEC. | $10^{-6}$ | 45000 ± 1% | 1000 SEC. |
| $10^8$ | $10^{-7}$ | 10 | 2.2 SEC. |
| $10^9$ | $10^{-8}$ | 10 | 22 SEC. |
| $10^{10}$ | $10^{-9}$ | 10 | 3.7 MIN. |
| $10^{11}$ | $10^{-10}$ | 10 | 37 MIN. |

Set the COUNT INTERVAL switch to $10^8$ and the ERROR RATE switch to $10^{-7}$. The display should reach a final count of ten. Setting the RCV ERRORS switch to PARITY will result in a final count of ten. Setting the RCV ERRORS switch to BIPOLAR VIOLATIONS should result in the detection of zero errors.

Now set the Transmitter's MULTIPLE ERRORS switch to BIPOLAR. The final error count should be ten. Move the RCV ERRORS switch to DATA and note that zero errors are counted.

Operate the transmitter SINGLE errors switch to DATA while the COUNT indicator is lit and note that a single data error is added to the display. Set the ERROR RATE switch to ERROR FREE and RCV ERRORS switch to BIPOLAR VIOLATIONS. Operate the transmit SINGLE error switch to BIPOLAR while the count indicator is lit and note the addition of a single error to display.

Set the MULTIPLE errors switch to $10^{-2}$. Note that a final count of zero is reached with the OVERFLOW indicator lit. Set the DISPLAY FORMAT switches for BLOCK SYNC and one second. The display should reach a final count of three. Set the switches for BLOCK ASYNC and two seconds. The final count reached should be a two. Set the SECONDS switch to nine and COUNT INTERVAL to $10^9$. The final count should be three.

Set the COUNT INTERVAL switch to CONT. Push and hold the STATUS switch while rotating each of the TIMER thumbwheel switches through all positions zero to nine. The number set on the switches should appear on the digit display.

Set the COUNT INTERVAL switch to TIMED. Set the TIMER switches to one minute and DISPLAY FORMAT switches to BLOCK ASYNC and one second. Push the RESET switch and wait for the count indicator to go out (Approx. 1 Min.). A final count of 60 $\pm$ 1 count should be reached.

2.2.7 **Errors - Print Mode** (if applicable)
Connect the Printer to a standard 115V AC, 50 - 60 Hz, single phase power source - Note that the DTR LED is lit.

Set these switches to the following positions:

| | |
|---|---|
| OUTPUT MODE | - to PRINT |
| COUNT INTERVAL | - to TIMED |
| TIMER THUMBWHEELS | - to 0-1-0 |
| SECONDS | - to 1 |
| BLOCK ERRORS | - to ASYNC |
| Transmitter, ERRORS MULTIPLE | - to DATA |
| ERROR RATE | - to $10^{-7}$ |

Momentarily depress RESET.

The display should read: -----P

The Printer is immediately activated and the following initial message is printed:

```
**********
   START

PRINT CYCLE          010M

SYSTEM STATUS

TEST PERIOD            00
  SIGNAL              OFF
  DS-3 SYNC           OFF
  DATA SYNC           OFF
  ALL 1'S             OFF
  BLUE DET            OFF
  POWER               OFF

TOTAL ERRORS
  BIT           000000000
  BPV           000000000
  PTY           000000000

BLOCK ERR-1 SEC
      E-S-A          E-F-S
BIT   00000          00600
BPV   00000          00600
```

Approximately 10 minutes after RESET, the following result should be printed out:

```
TEST PERIOD            01

TOTAL ERRORS
  BIT   000002727  (± 1%)
  BPV   000000000
  PTY   (indeterminate)

BLOCK ERR-1 SEC
      E-S-A          E-F-S
BIT   00600 (± 6)    00000  (± 6)
BPV   00000          00600
```

The printed output should be interpreted as follows:

```
**************
-                START
```

These two lines signal the beginning of a new test. They appear once per test. If a power failure occurs during the course of a test, these lines will be printed immediately when power is restored, thereby providing to the user an easy indication of the disruption. A new test will always be started following a power interruption.

```
-     PRINT CYCLE    xxxM
```

The number xxx on this line indicates how often (number of minutes) a printout will be provided. This number matches the duration of each test period, as selected by the operator through the MINUTES thumbwheel switches on the front panel.

```
-     SYSTEM STATUS


      POWER     OFF
```

These lines show the system status by providing to the user a printed copy of the states of the status LEDs on the front panel of the Test Set. The initial system status is printed at the start of a new test and an update is provided every time a change is detected. A single asterisk (*) will precede the new state of the LED where the change has occurred since the last update.

```
-     TEST PERIOD   01
```

Following RESET or after a power failure, a new test starts, which is divided into equal periods whose length is preset through the MINUTES thumbwheel switches. The Test Set buffers are cleared after each period, such that reported errors actually occur precisely during the indicated test period. A two-digit number is used to indicated the test period. Every 100 test periods, this number is reset from 99 to 00.

```
-     TOTAL ERRORS
```

This refers to the number of all individual errors in each category covered by the Test Set.

- BIT .....

The number of individual DATA bits found erroneous is printed on this line.

- BPV .....

The number of individual BIPOLAR VIOLATIONS is printed on this line.

- PTY .....

This line shows the number of individual PARITY BITS that are found to be in error.

- BLOCK ERR - xSEC

xSEC represents the size of a block of errors as selected for the test through the Seconds switch (1 thru 9).

- E-S-A E-F-S (Error-Seconds-Async Error-Free-Seconds)

Depending on the position of the BLOCK ERRORS switch, this line will read E-S-S E-F-S (for BLOCK SYNC) or E-S-A E-F-S (for BLOCK ASYNC). E-F-S refers to the blocks that happen to be error-free.

- BIT ----- -----

The number of DATA block errors and the number of error-free DATA blocks are printed on this line, respectively under ERR (or ERRED) and FREE.

- BPV ----- -----

On this line appear the number of BIPOLAR VIOLATIONS BLOCKS (under E-S-S or E-S-A) and the number of BLOCKS free of BIPOLAR VIOLATIONS (under E-F-S).

# 3.0 CONTROLS AND INDICATORS

## 3.1 Mode Select

### 3.1.1 OUTPUT MODE

The Bowmar Model 275B Transmission Test Set provides the user with the capability of outputting the results of a test either to a seven-segment LED display or to a printer.

With the OUTPUT switch in the DISPLAY position, errors accumulate on the 6-digit LED display according to the unique error type selected by the RCV ERRORS switch and the DISPLAY FORMAT group of switches. If the DISPLAY switch has been set to the HOLD position, at the end of the test, the number of errors of any type covered by the Test Set can be viewed on the display upon selecting this particular type through the switches indicated above.

If a printed output is desired, the following steps must be taken:

a) The OUTPUT switch set to PRINT,
b) The COUNT INTERVAL switch set to TIMED,
c) The desired test period set on the MINUTES thumbwheel switches. A minimum test period of 10 minutes is required, or the setting of the MINUTES switches will be flashed on the display.

After depressing the RESET switch momentarily, the following unique pattern will appear on the 6-digit display: ------P, signally the PRINT Mode.

When in the PRINT Mode, a test will continue indefinitely until interrupted by RESET or a power failure.

### 3.1.2 RCV ERRORS

A three-position switch which selects either DATA, PARITY, or BIPOLAR VIOLATION errors.

DATA ERROR -
The Receiver compares all received data, bit by bit, to its internal generator. Any discrepancy between them is recorded as a Data Error. Data Error checks cannot be performed on live traffic. One of the following sources must be used: Pseudorandom ($2^{15}$-1), All 1's (1111) or Short Patterns 1010 and 1100. The DATA ERROR mode of measurements are required when testing systems composed of equipment which remove bipolar violations.

**PARITY ERROR -**
The Receiver calculates parity for all data (information) bits within one frame and compares this result to the parity bits of the next frame code. Any differences between the two are recorded as a Parity Error. Any data message, including live traffic, properly framed with the DS-3 format is acceptable.

**BIPOLAR VIOLATION -**
The standard DS-3 carrier system defines a zero substitution code, B3ZS, which limits the number of consecutive zeroes present in the data stream. This code adds Bipolar Violations in a uniquely defined sequence so that the receiving terminal can return the data to its original form. The Test Set ignores these legal violations and records only those that do not conform to the B3ZS format. A violation is defined as two consecutive bipolar pulses of the same polarity.

### 3.1.3 FRAME

A two-position switch, DS-3 and UNFRAMED. Both the Receive and Transmit sections are affected.

In the DS-3 position, data from the transmitter's data generator is added to a standard DS-3 frame code. The Receiver separates the received signal into frame bits and data (information) bits. Both live traffic and the blue signal contain the DS-3 frame code.

In the UNFRAMED position data is transmitted without a frame code.

A FRAME is a uniquely defined code added to the multiplexed data which permits far end equipment to separate the multiplexed signal into separate channels. Additional frame bits define parity, fault signaling (XBIT), and bit stuffing.

### 3.1.4 DATA

Two switches are used to select the data pattern transmitted and received by the Test Set. The Transmitter cannot be instructed to send a data pattern different from the one the Receiver is set up to receive.

The first switch selects between PSEUDORANDOM and PATTERN. The PATTERN position activates the second switch which selects either 1111 (All 1's) or Short Patterns 1010 (Blue Pattern if Framed) and 1100. The numbers, 1111, 1010 and 1100, correspond to four bits of the actual data which are continuously repeated.

**PSEUDORANDOM -**
This pattern consists of 32,767 bits of data arranged in a defined sequence, which repeats. It conforms to an industrially accepted standard and is generated by a fifteen stage shift register with feedback to produce a $2^{15}$-1 bit word (32,767 bits). The energy content of this pattern closely resembles that of live traffic. Since the contents of this pattern is structured, it is possible to perform data error measurements with it which is not possible on live traffic.

**SHORT PATTERN -**
The Short Patterns consist of a group of four bits which are continuously repeated. The 1111, All 1's pattern, is useful for signal level calibration and measurements when transmitted unframed. The 1010 pattern framed is identical to the system alarm signal known as the Blue Pattern. The 1100 pattern contains the maximum number of consecutive zeroes permitted in a DS-3 system. Data containing more than two zeroes is restructured by the B3ZS code. Comparison of measurements taken with the three Short Patterns and the Pseudorandom pattern aid in resolving problems related to system pattern sensitivity.

## 3.2 Receiver

### 3.2.1 DS3-INPUT
A single compatible, 75 ohm, jack which connects the equipment under test to the Test Set's Receiver circuitry.

### 3.2.2 LEVEL
A three position switch which selects HI, LOW, DSX and NRZ input signal levels/formats. The HI/LOW position defines bipolar signal levels compatible with most terminal equipment. The DSX position permits connection to the system at a DSX-3 cross connect line jack. An auxiliary amplifier module is provided with sufficient gain to overcome monitor jack losses in a DSX-3 cross connect bay. The auxiliary amplifier adds sufficient gain to permit operation at receive levels between -22 dBm and -33 dBm. the NRZ, Non-Return to Zero, position selects system data and clock connected to the Test Set's optional NRZ modules' RCV ports. Either of two modules are available: One a 75 ohm $\pm$ 1V, the second a 50 ohm -0.9 to -1.8V interface. The modules are field interchangeable and mount in place of the auxiliary amplifier module.

## 3.3 Transmitter

### 3.3.1 DS-3 OUTPUT

Six independent but equal bipolar outputs capable of fully loading M34 multiplexer, fiber optic or radio equipment. A delay is provided which will shift the data pattern at the sixth (lower) jack eighteen time slots behind the other five.

### 3.3.2 LEVEL

A three position switch which sets the six output jacks to one of three standard signal levels: HI, LOW, DSX. Transmit outputs located on the NRZ module are always active.

### 3.3.3 ERRORS, ERROR RATE

Three switches, MULTIPLE, SINGLE and ERROR RATE permit the controlled insertion of either data or bipolar violations into the transmitted data. The MULTIPLE switch selects DATA or BIPOLAR errors inserted at a rate determined by the ERROR RATE switch. Error insertion is discontinued in the ERROR FREE position of the ERROR RATE switch. A red indicator is lit for all switch positions except ERROR FREE. This visual indication reduces the chances of inadvertently inserting errors. The SINGLE errors switch is a two position momentary action type. When moved to the DATA position a single data error will be inserted. Likewise, in the BIPOLAR position a single Bipolar error is inserted. When released, this switch returns to a neutral, center, position.

A Data Error represents an inversion of one data (information) bit from a true state to its unwanted complement. Data Error insertion is limited to the data field only and will not effect frame code bits. Insertion occurs after transmit parity is calculated resulting in the production of a corresponding parity error.

A Bipolar Error is inserted by forcing two consecutive bipolar pulses to the same polarity. Bipolar error insertion is restricted such that it will not violate the zero substitution code, B3ZS. This insures that Data Errors will not be created by Bipolar Violations.

### 3.3.4 X BIT

A rear panel switch which set the X BITS in the frame code to the alarm status of 11 when depressed.

## 3.4 Receiver Status

### 3.4.1 X BIT

One yellow indicator which is lit whenever the X-BITS within the received frame code are a logic one.

### 3.4.2 SIGNAL

One active (yellow) and one history (red) indicator which identifies the absence of data at the Receiver's DS-3 INPUT. The History indicator is lit whenever the signal was lost and regained. This indicator is reset by either RESET HISTORY or RESET switches.

### 3.4.3 DS-3 SYNC

One active (yellow) and one history (red) indicator. When lit, the Test Set's Receiver is unable to acquire frame synchronization. The yellow indicator is forced on when the FRAME switch is set to the UNFRAMED position. The history indicator is reset by either the RESET HISTORY or RESET switches.

A frame code is added to multiplexed data channels by the originating equipment to provide a process which is used by the far end receiver to identify individual channels. The process, synchronization, is implemented by searching for and identifying a sequence of bits within the frame code defined as F-BITS and M-BITS. Frame synchronization is a two part process which first finds the F-BIT sequence and then searches to recover the M-BIT sequence. Once synchronization is established it is possible to separate frame code bits and the data pattern.

### 3.4.4 DATA SYNC

One active (yellow) and one history (red) indicator which is lit whenever the Receiver's data generator cannot align itself with the received data. Data Sync must be acquired before data errors can be identified. The History indicator is reset by both the RESET HISTORY and RESET switches.

### 3.4.5 ALL 1's

One active (yellow) and one history (red) indicator which is lit whenever the received data consists of at least on thousand consecutive ones. The History indicator is reset by either the RESET HISTORY or RESET switches.

### 3.4.6 BLUE DET

One active (yellow) and one history (red) indicator which is lit whenever a Blue Signal is detected at the test Set's input. The History indicator is reset by both the RESET HISTORY and RESET switches.

3.4.7 **POWER**

One history (red) indicator which is lit whenever power is momentarily interrupted or the test Set is turned on. To reset use either the RESET HISTORY or RESET switch.

3.4.8 **RESET HISTORY**

A pushbutton switch which when pressed will reset all history indicators without interrupting a test in progress.

3.4.9 **RESET**

A pushbutton switch which resets all Test Set circuitry, display and history indicators. A new test begins at the release of this control.

3.4.10 **DISPLAY Switch**

A two-position switch, 10 SEC and HOLD, controls the automatic start of new test periods. In the 10 SEC position the final result of a test will remain on the three digit display for approximately ten seconds before a new test is started and the display is cleared. The HOLD position prevents new tests from starting and maintains the result of the last test until the RESET switch is pressed. This position should always be used when making a timed test or for long count intervals of $10^{10}$ and $10^{11}$ bits. This permits the operator to leave the test set unattended during the test run.

3.4.11 **OVERFLOW, COUNT and DIGIT DISPLAY**

The DIGIT DISPLAY consists of six seven-segment type LED digits. Errors are added to the display at the moment of detection. The displayed errors are read as total errors per number of bits, seconds or minutes. Measurements defined in Error Rate must be calculated by dividing the total number of errors detected by the length of the measurement period in bits.

The OVERFLOW indicator illuminates whenever the maximum capacity of the DIGIT DISPLAY is exceeded (999999). This indicator is cleared by the RESET switch.

The COUNT indicator is lit during a test measurement period as defined by the COUNT INTERVAL switch and is extinguished coincident with the end of a test.

### 3.4.12 COUNT INTERVAL

The COUNT INTERVAL switch determines the length of a test period.

The TIMED position activates the TIMER which provides a selectable test length of 1 - 999 minutes in one minute steps. The equivalent number of bit intervals may be calculated by multiplying the number of minutes selected by the constant, $2.68 \times 10^9$.

The CONT position provides a continuous or endless test period. This period is started or re-started by the RESET switch which also clears the display. Positions $10^8$ - $10^{11}$ select bit intervals. Positions 1 Sec. - 1000 SEC. select actual time intervals in seconds. The $10^9$ position requires ten times as long as the $10^8$ position or 22 seconds, $10^{10}$ requires 220 sec. = 3.7 min. and $10^{11}$ requires 2200 sec. = 37 min.

### 3.4.13 TIMER

The TIMER consists of three thumbwheel switches and a pushbutton switch, STATUS. The thumbwheel switches set a test interval of 1 to 999 minutes in one minute steps. The COUNT INTERVAL switch in the TIMED position activates the timer function. Pressing the RESET switch starts the timed test period. Resetting the Test Set before the completion of a TIMER interval will clear the display and start the test from the beginning.

### 3.4.14 STATUS

In the DISPLAY mode of OUTPUT, the time remaining to test completion can be observed on the three least significant digits of the display by pushing the STATUS switch. This does not affect the test in progress.

This switch takes on a different function in the PRINT mode. When depressed, it will trigger an immediate printing of current system status data (including error accumulation), provided that the time to test period completion is at least two minutes.

### 3.4.15 DISPLAY FORMAT

The DISPLAY FORMAT group consists of three switches: ERRORS and SECONDS on the front panel, and BLOCK ERRORS on the rear panel.

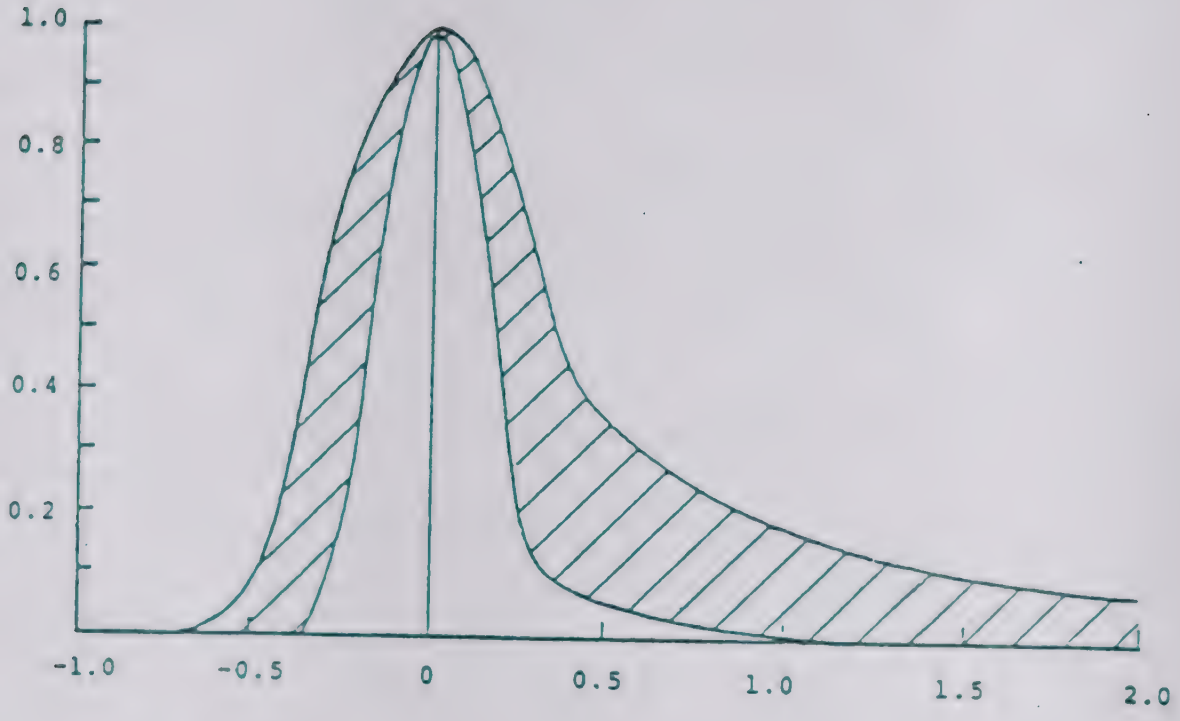
The ERRORS switch selects between SINGLE errors and BLOCK errors. In the SINGLE errors position, every error detected by the receiver circuitry is accumulated on the 6-digit display. The BLOCK position activates the BLOCK ERRORS switch. In the BLOCK mode, individual detected errors are formatted into blocks whose length is

Buffers Q15, 16 are emitter followers which present a buffered B3ZS signal to output drivers Q10 - Q14, Q17. These drivers with output resistors R65, 68, 71, 74, 77, 109 source 75 ohm at .9V or .18V peak when front panel XMT switches are set at HI or LO respectively, Resistor R10 is a select from 0 - 100 ohms at HI XMT levels. Resistor R101 is a select from 150 - 250 ohms at LO XMT levels.

If DSX is chosen as the XMT pattern via front panel switches then relay K2 is closed. L6, C42 with resistors 89 - 93 simulate a line build out circuit of 450' at T3 rates. Refer to attached pulse template, Figure 4-1. The signal from this point is buffered exactly as above. DSX data is now presented at the six outputs. If Option 01 is chosen, R106 is deleted and R107 inserted. Shift registers U16, 17, 23 delay the output bit stream by 18 bits before outputting the information to Q17 via Q18. Bipolar positive data (bipolar +) is similarly delayed 18 bits via ICs U21, 22, 24. Another 1/2 bit delay arises from the phase of XMT clock inputted to U19a-b which is opposite that inputted to U12a-b. This totals 18 1/2 bits or the 19 Bit Delay Option 01. Circuitry is identical to that of the buffer described above. Relay K3 is closed when DSX is selected and delayed data is output at the bottom jack on the front panel. All other 5 jacks are not delayed.

Received B3ZS Data is sent initially to this module for processing. Data is inputted on J1 and sent (via Relay K1) to a differential gain stage comprised of transistors Q1, Q2 and constant current source Q3 with external components. Resistors R1 - R5 with capacitor C2 and inductor L2 form a 450' equalizer which are selected via K1 and front panel switches (DSX RCV). R8/R7 and R9/R10 set up an AC gain of 6 presented at the Q1, Q2 collectors. Resistors R13, 14 are a resistor divider network which set up a constant current of 26 mA through the C-E region of Q3. Amplified data is sent to peak detector input Q4. In this circuit, as long as the input voltage is increasing, diode Q6 is conducting. The Q4, Q5 amplifier is in the voltage follower mode and the output presented at C13 follows the input. U1a is a voltage follower in the feedback loop and serves to isolate the capacitive load from amplifier input. The peak result is attenuated by 1/3 through U1b and resistively coupled R30-31 to sampling circuit U2-U3 where data is sampled at approximately 2/3's peak value and translated to ECL levels at the inputs of gates U4a, b, d.

## DSX-3 ISOLATED PULSE TEMPLATE




TIME SLOTS - NORMALIZED TO PEAK LOCATION

FIGURE 4-1

Recovered clock is generated from the incoming stream of 44.736MHz B3ZS data (U5 Pin 4). L3-C22, C100 and L4-C23, C101 formed a capacitively coupled (C21) bandpass filter for a center frequency of 44.736 MHz. The loaded Q of the circuit is approximately 10 which guarantees flat passband and deep skirts. C22, 100 will adjust the overall shape of the outputted clock at TP1 whereas C23, C101 will adjust the phase as to center it on RCV Data + and RCV Data -.

4.2 Code Module - A2

Data to be transmitted is coded and Data RCV is decoded on this module. Individual data errors are first added to the XMT Pattern through Latch U12. CK data is used so as not to error a frame position. The error frequency and type is decoded through gates U17c-d via front panel switches.

Data is coded with B3ZS code through a complex look ahead design involving U25 latches and external gates. Latch U22b with gates U23b and U18c are an odd/even counter which reset to even after a B3ZS error (U23 Pin 10) or V-Bit (U23 Pin 11) is inserted (Ref. Table I). U23c creates the data pattern to be transmitted; Pin 12 becomes HI for a V-Bit time, Pin 14 is a B-Bit (Ref. Table I), Pin 13 is the data pattern to be XMTed before coding. B-Bits will be HI if the even/odd counter inputs an even parity (LO) to U19b. Latch U22a with gate U23a create the bipolar positive data bit times when U22a is set. This latch is disabled from changing state at V-Bit occurrences via U23 Pin 5.

B3ZS errors can be inputted through latch U14a. The error state (HI) is set until U19a is enabled. U19a is enabled after even parity is detected on a "Real" data bit. Then the next "Real" data bit is inverted via U23a and U22a. This gives an even number of pulses between violations (Ref. Table I - Fig. 4-2) and consequently an error.

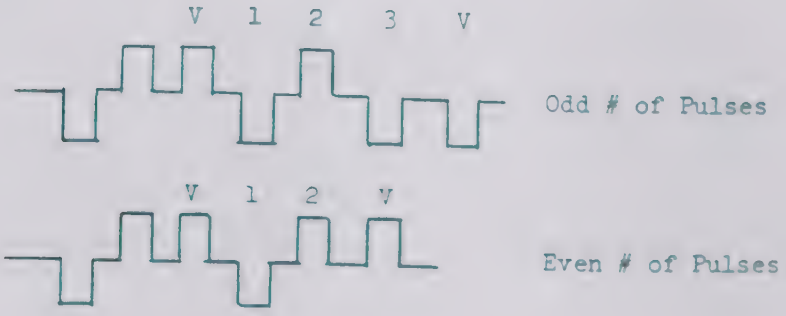



**FIGURE 4-2**

RCV data is decoded conversely through a very simple technique involving J-K latch U8 and external gates. One violations pair will result in a LO on U4 Pin 14. This enables U5d to invert a V-Bit position and U4a to make LO a B-BIt position. Two violation pairs of the same polarity in a row result in a HI on U1 Pin 14, and therefore a B3ZS error. Any B or V-Bit change is now prohibited via U4 Pin 7. Decoded data and B3ZS errors are latched by U7. Decode circuitry U3 with latch U6 and enternal gates select the data to be analyzed (NRZ or B3ZS) via front panel switches. The B3ZS decode circuitry above is disabled if NRZ pattern is selected by setting latch U8 via a front panel switch.

The Error Rate Clock is generated on this module. ICs U27 - 35are a string of divide by 10 counters which create the different rates. The output (U26b) is selected via front panel switches and decode logic U27, U26a, c.

BNC outputs of this module are buffered by U15, U20 and U10c before being output. BNC input (EXT Clock) is 75 ohm ECL compatible and buffered by U10a-b.

TABLE I

ILLUSTRATIVE EXAMPLE OF B3ZS CODING

Binary Signal: 10100011000000010001

| B3ZS Signal | | Odd B=0 | Even B-1B=1 | | Odd B=0 |
|---|---|---|---|---|---|
| | | \| | \| \| | | \| |
| Case 1 (Odd) | +0-00-+-+0+-0-00+00+- | | | | |
| Case 2 (Even) | +0-+0+-+-0-+0+00-00-+ | | | | |

In the B3ZS format, each block of three consecutive zeros is removed and replaced by B0V or 00V where B represents a pulse conforming with the bipolar rule and V represents a pulse violating the bipolar rule. The choide of B0V or 00V is made so that the number of B pulses between consecutive V pulses is odd.

This example of B3ZS coding assumes the polarity of the last pulse transmitted was -. If the last pulse transmitted had been +, then the resulting bipolar signals would be the inverse of the example shown here. Case 1 assumes that an odd number of pulses have been transmitted since the last bipolar violation.

FIGURE 4-3

## 4.3 F & D Module - A3

The F & D (Frame & Data) Module DS3-203 is inserted into two slots in the 275 card rack. One slot corresponds to the XMT function (Slot 3). The other slot corresponds to the RCV function (Slot 4). The module is designed to work in either mode and therefore is used identically in both slots.

### 4.3.1 F & D XMT

When inserted into Slot 3, the XMT mode of the module is automatically chosen. In this mode data is generated and a frame pattern inserted. This Data Mux pattern is sent to the Code Module (via motherboard) for further processing.

Data can be one of four switch selectable patterns (front panel). ICs U2, 3, 4, 5, 7, 8, 9 create the four unframed patterns which are inserted into 4 x 1 Mux U6. Front panel data select switches are directly connected to the select Pins 7, 9 of U6. Actual data chosen is seen at U6 Pin 2. The QRSS ($2^{15}$-1) pattern is generated by a 15 stage shift register (U8, 4, 3a-c) with feedback provided by U7a-b. In the XMT mode of operation, U8 Pin 15 is directly connected to U4 Pin 5 via U5a-b. IC U2 provides false start security in that if 15 logic zeroes are seen shifting through the generator (U8, 4, 3a-c) the next bit inserted is inverted, sending an invert level to U7-a. U2 serves another function in that 14 zeroes in a row are seen once every $2^{15}$-1 bits when the QRSS generator is in normal operation. U2 with decoding circuitry U1 (a-d) recognizes this 14 bit zero pattern and XMT a pulse (word sync) when detected. 1100 data is generated by the 2 stage register U3 (d-e) with feedback provided by U9(d). 1010 data is generated by the 1-stage generator U3(f) with feedback provided by U9(a). The phase of the 1010 pattern is controlled by U16 (3). This insures that a logic 1 will follow a frame slot when the 1010 pattern is transmitted.

U16, U18 and U19(d) form a divide by 85 counter which control frame bit insertion (CK frame). U24 is disabled in the XMT mode. U31 - 32 create the control circuitry for each subframe (8 frame slot times). U32 Pin 1 controls M-Bit insertion. U32 Pins 2, 9 control F1-Bit insertion. U32 Pins 3, 5, 7 control C-Bit insertion. F-Bits are constant from subframe to subframe and do not require any more control circuitry. C-Bits are constant for 7 subframes (1 complete frame) and then are updated from the C-Bit generator (U34, 35, 33a, c). U34a-b and

U33a-c produce a repeatable 001 pattern. U35 inverts the center data bit every 6 patterns to produce a ... 001001001001001011001 pattern (every 18 frames a C-Bit is inverted).

M-Bits are generated by decoding circuitry U29, U30, U26, U27a-b. All M-Bits are summed at U20 Pin 14. Parity is calculated each complete frame (excluding frame slot locations) by an odd/even counter (U13a-b-c, U14a-b) and latched at the end of a frame by U15b. Parity is inserted into frame locations M3-4 (U20d) in the next frame. F, C, and M-Bits are summed together at U20 Pin 2 and sent to sampling circuitry U10-b. U10a-d multiplex data with frame and XMT the result (Mux Data).

4.3.2 **F & D RCV**

When inserted into Slot 4, the RCV Mode of the module is automatically selected. Operation in this mode is exactly the same as in Slot 3. Initially Loop Control (Pin 96) is held low externally. This forces incoming data into the data generators (U3, 4, 7, 8, 9), which quickly synchronize with incoming data. Loop Control is then forced closed (HI) and operation is exactly the same as in the XMT Mode.

Frame Synchronization is independent of Data Synchronization. F-Bit sync is first looked for bit by bit through adjust circuitry U24a-b. CK Frame (U18 Pin 15 is continuously adjusted until F adjust pulses are no longer seen at U24). Simultaneously M-Bit sync is checked. Counter U29 is forced ahead one M-Slot every frame until M-Sync is found (Pin 3 of U29, when HI, begins its count at 0001 rather than the 0000 normal position). IC U21 contains 6 independent latches useful only in the receive mode (Slot 4). F-Bit and M-Bit control circuitry is latched and sent to the Sync Module where F-ADJ and M-ADJ pulses are generated.

4.4 **Sync Module - A4**

RCV Data is directly sent to the Sync Module (Slot 5) where data and frame comparisons are made. Generated RCV Data U7 Pin 4 is created at the frame and Data Rcvr (Slot 4). Timing is critical. U8a delays the RCV data to match the generated data in phase. Latch U8b samples data comparisons of U7 Pin 2 and latches on an error. Latch U8b is prohibited from latching on frame slot errors because its clock input is "gapped" (CK Data) at a frame slot location. Lost Data Sync is statistically defined as 1024 individual errors in 32,767 bit comparisons. Counters U3, U4, U5 detect and count errors up to a 1024 ($2^{10}$) count, then U5 Pin 15 signals U1b that data sync is lost. U3, U4, U5 are automatically reset every 32,767 ($2^{15}$) data slots by an external reset pulse

(Word Sync) generated on the F & D RCVR Module. Once Data Sync exceeds threshold, U1b latches and sends an "Open Loop" command (U1 Pin 15) to the F & D RCVR. Error Counter (U3 - U5) is disabled during this time through U6 Pin 9. U1a with U2 count data comparisons. When 30 "good" sequential data comparisons are detected, U2 overflows and commands U1b to set (close RCVR Loop). U2 is prevented from overflowing and reset if any data error is detected during this time by U8b's latch output. Data will acquire synchronization only on the 4 switch selectable patterns.

RCV Data U7 Pin 14 is compared against a RCVR generated frame pattern U7 Pin 15 created on the Frame and Data RCVR (Slot 4). Latch U17a samples the result of F-Bit locations (CK F-BIT). Lost F-Bit Sync is statistically defined as 3 bad F-Bits received in 15 compares. Counter U35 counts F-Bit errors. A count of 3 will set latch U22b, and cause counter U29 to look for 15 "good" compares in a row before overflowing and resetting U22b. U22b will be relocked LO every 15 F-Bits through U34a as long as 13 of 15 F-Bit compares are correct. F-ADJ pulses are sent to the F & D RCVR for every occurrence of an error when U22b is set (U30c, U34c).

M-Bit Sync is searched for simultaneously (but in a much greater time interval). M5-M6-M7 will always be transmitted at levels 0-1-0, respectively. Lost M-Bit Sync is statistically defined as 2 bad M5-M6-M7 compares in 3 frames. Latch U16a samples the result at M5-M6-M7 locations (CK M5-7). Counter U21a-b counts M5-7 group errors. A count of 2 will reset U21b and set latch U22a. U26c is now enabled and M-ADJ pulses are automatically sent to the F & D Receiver for every occurrence of an M5-M6-M7 error. To set counter U21, U27 must count 3 error free M-Bit compares in a row. If M-Bit Sync is not found in 15 frames, counter U28 overflows and forces an F-ADJ pulse by setting U22b on the next F-Bit reclock. (U28 is reset when U22b is set).

Latch U16b samples the Parity Result at M3-M4 locations (CK M3-4). An error will set U16b. U16b is reset before another error evolves by CK M5-7. In this way a pulse is generated for each parity comparison error per frame.

Detected Data and Parity Errors are forwarded to the Timebase Module for further processing. B3ZS errors are detected on the Code Module (Slot 2), from where they are similarly transmitted to the Timebase Module.

All Ones condition is detected by counter U13 with one shot scheme U25a,b. U13 is normally counting with Pin 14 changing state. With this condition, IC U25 is

continuously pulsed and keeps U31 Pin 8 at a Logic HI. If 1000 ± 100 data bits are sequential 1's (22 usec), U25a changes state and forces U31c into an All 1's state. This state is guaranteed for 200 ms ± 25% by U25b. Blue Pattern (U9, U24) is detected in exactly the same manner with data comparison on U7c.

RCV CLK is injected into divide by 10 counter U15. As long as CLK is inputted, Q20a is set. If clock is not inputted for 100 pulse times, U20a is reset and held in this state for 200 ms ± 25%. This denotes signal loss and receive clock is generated by continuous data pulses. A signal loss condition forces LED Blue, and LED All 1's to an off condition (U31 Pin 9 - U23 Pin 1), also LED DS3 Sync and LED Data Sync are forced on (LO) (U31 Pin 11, 3).

If M-Bit Sync or F-Bit Sync are lost, U33a is forced on (Latch LO) for 200 ms ± 25%. This will denote DS3 Sync lost. If loop control is open, U33b is forced on (Latch LO) for 200 ms ± 25%. This denotes Data Sync lost on front panel LEDs.

## 4.5 Timebase Module - A5

The Timebase Module, with its 8035 CPU, decodes timebase, count interval, output mode and display format switches from the front and rear panels. It also manipulates the detected errors, and sends the result to the Display Module or the RS232C Printer Interface, as selected by the user.

Individual errors detected by the SYNC and CODE modules are forwarded to the Timebase Module for processing.

Parity errors are inputted through U8 and are counted by the four-decade counter 0 of U14, which is cascaded by software with four more decades obtained by using two 8-bit registers from the on-chip RAM of the 8035.

Individual Data errors are counted by U6 cascaded with counter 2 of U14 and two RAM registers on the 8035, forming a 9-decade counting chain.

Similarly, single Bipolar Violations are monitored through counter U1 along with counter 1 of U14 and two internal registers of the 8035, thus providing a $10^9$ counting capability.

Block of Data Errors are counted by monitoring U7 Pin 12 (DATBLK) and interpreting each change of state as the occurrence of a new block error. Blocks are formed by the D flip-flops of U5 in combination with the exclusive-OR gate U10b, the multivibrator U18b and

counter 2 of U17 used as block timer. U7 and U9 provide ECL-to-TTL and TTL-to-ECL conversions respectively. The same circuit elements are used to implement both BLOCK SYNC and BLOCK ASYNC. In the BLOCK SYNC mode, a block is started following the detection of an error by U5a, which causes a trigger to the multivibrator. Approximately 2 ms later, counter 2 of U17 is in turn triggered by the rising edge of the negative pulse on U18b Pin 12. A negative pulse on U17 Pin 17 is then started which will last for the number of seconds set on the Second thumbwheel switch. No change in the state of DATBLK is allowed for the duration of this pulse, since the outputs of U5b are prevented from changing by holding the clock input LOW. On the rising edge of the pulse, which marks the end of a block, the output of U5a is transferred to U5b, and a new block is allowed to start with the occurrence of the next individual Data error. In the BLOCK ASYNC mode, the circuit operates in a similar manner, except for the following:

- the CLEAR input of U18b is active, which holds HIGH the GATE input of counter 2 of U17;

- each block is started not by the occurrence of a DATA error, but rather at precise instants determined by the rising edge of the clock input of U5b;

- counter 2 of U17 is operated in a different mode: instead of remaining LOW for the duration of a block, output OUT2 of U17 remains HIGH for the first half of the block and then goes LOW for the second half. This process is repeated continuously, providing a rising edge for the clock input of U5b at the beginning of every new block.

Blocks of Bipolar Violations are counted in an identical manner, using the D flip-flops of U4, the exclusive-OR gate U10a, the multivibrator U18a and counter 1 of U17 operated as a block timer. As for the DATA Errors, U7 and U9 provide ECL-to-TTL and TTL-to-ECL conversions.

Each test period is measured by counter 1 in cascade with counter 0 of U23. When the Count Interval is specified in seconds, counter 0, loaded with 45, provides an input pulse to counter 1 every 0.1 second. The setting of the Count Interval switch is then multiplied by 10 and loaded into counter 1. This provides a means of approximating the test interval as closely as possible with the 0.0022 sec. clock from the Code Module. With the Count Interval specified in bits, counter 0, now loaded with 100, provides an output pulse to counter 1 every 0.22 sec. or $10^7$ bits, e.g. if the specified count interval is $10^8$ bits, counter 1 is loaded with $10^8/10^7$ or 10. When the

count interval is specified in minutes, counter 0 is loaded with 27273 to provide a pulse to counter 1 approximately every minute. Counter 1 is initially loaded with the setting of the Minutes thumbwheel switches. For any unit used to specify the Count Interval, output OUT1 of counter 1 will go LOW to mark the beginning of a test period. It will go HIGH and interrupt the 8035 CPU upon expiration of the test interval. When the Count Interval switch is in the CONT position, Pin 31 of U30 (CONT), is driven LOW, holding Pin 11 of U13 (STOP TEST) HIGH, thereby preventing any interrupt to the CPU and keeping the test enabled until stopped by RESET.

Counter 2 of U23 uses the 2 MHz T0 clock from the 8035 CPU to generate the Baud Rate (110/300) for the 8251A UART (U29) used in conjunction with the U32 driver and the U21 receiver to implement the RS232C interface to the printer.

IC U30 is an 8-bit CPU with a 64-byte on-chip RAM. It controls all data transfers on the main Data Bus ($DB_0$ $DB_7$) and on the 4-bit mini-bus ($P_{20}$ - $P_{23}$). Communication with the 7-segment LEDs on the Display Module is provided through the U24 and U27 drivers. Since the 8035 CPU features a multiplexed address/data bus, the 8212 Address Latch (U28) is used to capture the eight lower bits of the address bus when outputted by the CPU. The address generation coincides with the falling edge of the ALE signal, which is used to strobe it into U28. Similarly, the mini-bus carries time-multiplexed address information for memory as well as address and data for the 8243 I/O Expanders. Thus, an 8212 IC (U19) is used to latch the upper address bits intended for memory.

IC U31 is a 4K x 8 EPROM which provides the memory space needed to support various functions in software. IC U25 is a 1-of-16 decoder which uniquely selects each peripheral chip for data transfers to and from the 8035 CPU. ICs U11 and U15 are 4 line-to-16 line I/O Expanders which allow the CPU to easily monitor various switches and LED indicators off the Timebase Module, as well as to provide control for and read status of on-board peripheral components.

The 6 MHz crystal (Y1) is used in conjunction with the on-chip oscillator of the 8035 to provide timing information for all the CPU functions. A 2 MHz clock (T0) is also derived from the crystal frequency and used by counter 2 of U23 to generate the baud rate for the 8251A UART.

The E1-E4 straps allow to choose the printer baud rate of 110 or 300. For better resolution in the Block Error count, the 300-baud rate is provided as standard, unless otherwise requested.

4.6 **Power Supply Pan**

The Power Supply Pan consists of the A9 and A13 modules. These modules supply plus 5V and minus 5.2V to all logic modules.

The A9 module creates a +5V, 3 amp supply on J9 Pin 5. Diodes CR2, 3 full wave rectify the secondary voltage of T1. C1 is an enormous filter with regulator VR1 which supply +5V to all logic with less than 100 mV ripple.

The A11 (off-line switcher) provides a -5.2V at 9 amps to all logic boards. Ripple is less than 100 mV. Adjust resistor can vary the DC output from 4.8V to 5.2 VDC.

The A16 (off-line linear supply) provides $\pm$ 150 mA to the RS232C line drivers (U32). Ripple is limited to 2 mV P-P max.

IC U1 of A9 is an 8V Voltage Monitor. Front panel reset switch is directly connected to Pin 1 which sets this R-S latch when LO. When the potential between U1 Pin 11 and 13 is $\leq$ 8 VDC transistor Q1 is open and presents a reset condition to Latch U2 (Power LED on).Only after subsequent reset from the front panel switch will this latch be set.

4.7 **5-7V Regulator - A12**

Variable outputs of 5 to 7 Volts, 400 mA sent to Interface Module A1 via motherboard. Resistor R1 adjusts the voltage out at a minimum ripple 100 mV under full load. CR1, 2 are a full wave rectifier and C1 with VR1 represent a 5-7 volt, 400 mA regulator.

4.8 **Timer Module - A7**

In the TIMED Mode, the setting of the Minutes thumbwheel switches is read by the 8035 CPU, which uses this data to load the test period Timer. The outputs of these switches are pulled up by R6 - 11 & R15 - 20.

Similarly, the data from the Second thumbwheel switch is loaded by the CPU into the block timers on the Timebase Module. The outputs $2^0$ - $2^3$ of this switch are pulled up by R2-5.

U1 is a 4 line-to-16 line I/O Expander which provides a convenient and economical way to interface these switches to the 8035 CPU.

4.9 **NRZ Module - A10**

(Selected by the 2753-1 Option)
ECL Data and CLK XMT are converted to ± 1V, 75 ohm, transmit signals. Line receiver U1A differentially drives Q1, Q3 base. Transistor Q7 with Resistor Dividers R3, R31, R7 establish an approximately 35 mA current source. Transistor Q5 with Resistors R15, R13, R33 establish an approximately 70 mA current source. When Q3 is conducting, 70 mA are pulled from collector to emitter. When Q3 is cutoff, 35 mA is being supplied to E3. This ON-OFF transistor technique established ± 1 volt levels at a 75 ohm load across E3-E4 junction. This technique is repeated for the XMT CLK signal U2a, with current source provided by Q6 and Q8.

RCV Data is input into a resistor divider formed by R25, 27, 29. The AC impedance is 75 ohm. The resistors were chosen so as to center the data input into U1b around VBB. This technique is repeated for RCV CLK signal U2b, with resistor divider formed by R26, 28, 30.

4.10 **NRZ Module - A11**

(Selected by the 2753-2 Option)
ECL XMT Data and CLK are buffered by U1a, U2a and U1b, U2b, respectively. Outputs are ECL 50 -75 ohm compatible. ECL RCV Data and CLK (75 ohm) are inputted via Line Receiver U1c-d, respectively.

4.11 **Display Module - A8**

Signal, DS-3, DATA, ALL 1's, BLUE DET and POWER LEDs are driven directly from the Sync (A4) and Power (A9) modules. When a "Loss" condition occurs, DS5, 7, 9, 11, 13 or 4 will turn ON. When a "Good" condition is restored, DS6, 8, 10, 12, 14 will latch to an ON state (U5b, U3, U4). 10 x 4 encoders U6 and U7 effectively reduce the number of interconnections from 20 to 8 for the COUNT INTERVAL and ERROR RATE switches, respectively. CR2-5 effectively create ECL HI and LO levels from S4, S9 switch positions. U1 and U2 are BCD-to-7 segment display decoders/drivers which drive the 6 7-segment LEDs, DS16-DS17 and DS18-21 respectively, under the control of the 8035 CPU.

4.12 **DSX Monitor Module - A15**

(Selected by the 2753-3 Option)
IC U1 with Q1, Q2 provide automatic gain to a DSX3 signal input between -20 and -33 dBm. Q3 with filter R12, C13 form a peak detector whose result controls the gain of U1 via Pin 2. Q1 has a fixed AC gain of 13 and Q2 is an emitter follower buffer output.

## 5.0 CALIBRATION

5.0.1 To perform Test Set calibration it will be necessary to remove the outer case.

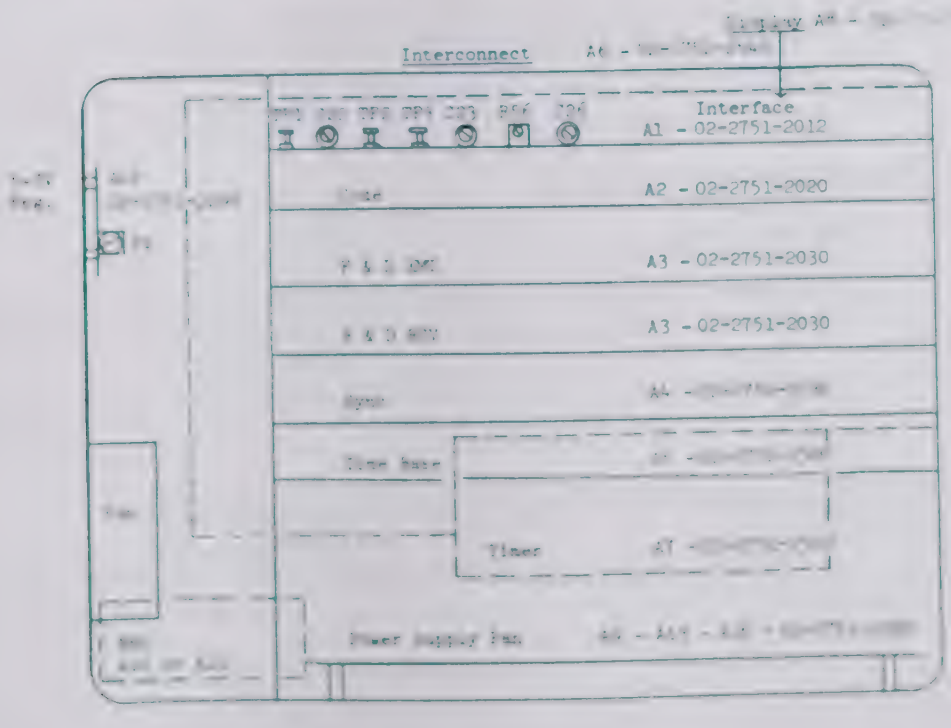
**CAUTION:** Be sure power cable is disconnected from Test Set before proceeding.

The outer case is held to the inner chassis by ten No. Six Phillips-head screws. Remove all screws completely and pull unit from case using the two front panel handles.

It will be necessary to apply AC power to the unit in order to perform calibration. The unit should be connected to a 3-prong AC outlet to insure proper chassis to earth grounding. A shock hazard exists in the area surrounding the fuse, power switch, and fan.

Connect the Test Set to the 60 Hz, 110V line via the line cord provided. Turn the power switch on, which will light its internal lamp. The test set should be powered for approximately 30 minutes before calibrating.

5.0.2 **System Architecture**



5.1 **Test Equipment**

a. Frequency Counter - 7-digit, 50 MHz minimum

b. Oscilloscope - Tektronix 7000 series or equivalent

c. Trumpeter Jumper (output-input)

d. (2) 75 ohm (RG59U) Cables - NRZ Option 1 Only

e. Trumpeter cable that mates to scope and is terminated 75 ohm to ground.

f. 75 ohm, 20 dBm attenuator (DSX Monitor Option Only)

5.2 **Transmitter Calibration**

5.2.1 a. Connect (e) from DS3 output 1 to Scope.

b. Adjust R1 on System Architecture for minimum rise and fall times (4.4 ns ± 1.5).

5.2.2 **Crystal Oscillator 44.736 MHz**

a. Connect CHANNEL 1 Probe of Scope to TP3. Observe a 44 MHz squarewave.

b. Connect Frequency Counter to rear of scope (CHANNEL 1) and increase Volt/Div. to 100 mV/Div. - AC select.

c. Adjust C26 for a 44.7360 MHz ± 100 Hz reading.

d. Adjust R56 until a 50% duty cycle is seen (tune R56 for maximum cycle 45 - 50% is acceptable).

5.3 **Receiver Calibration**

5.3.1 **Clock Recovered**

a. Connect CHANNEL 1 Probe of Scope to TP1. Connect CHANNEL 2 Probe of Scope to TP2. Sync on CHANNEL 1.

b. Set Front Panel Switches at QRSS select, DSX XMT and RCV. Loop back DS3 output 6 to DS3 input. Framed Mode.

c. Observe a QRSS ECL pattern on TP2, CH.2.

d. Tune C22 until a 44 MHz squarewave is seen on CHANNEL 1.

e. Adjust C23 until CHANNEL 1 clock centers CHANNEL 2 data.

f. Readjust C22 for 50% duty cycle and maximum focus.

g. Repeat e - f, if necessary. CHANNEL 2 Probe on TP3. Sync on CHANNEL 2. Observe no jitter on CHANNEL 1.

h. CHANNEL 2 Probe on TP2. Sync on CHANNEL 1. Connect frequency Counter to rear of scope (CHANNEL 1) and increase Volts/Div. to 100 mV/Div. - AC select. Register a 44.736 MHz ± 100 Hz register.

j. With XMT/RCV LEVEL switches set at DSX switch through all four data patterns and notice that CHANNEL 1 centers CHANNEL 2 ± 2 nsec.

k. Repeat j with XMT/RCV LEVEL switches set at LO.

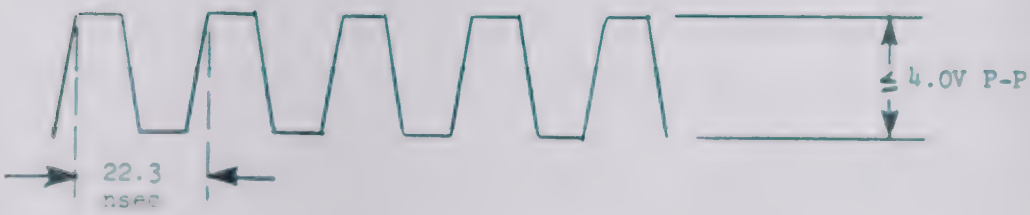
l. Repeat j with XMT/RCV LEVEL switches set at HI.

5.3.2 Repeat Section 5.3.1 (j - l) with DS3 output 5 looped back to the DS3 input.

5.4 NRZ Module - Option 1

Remove NRZ Module from main frame. Do Not disconnect 14 Pin connector.

a. **OPTION 1 - A10 Board**
Jumper BNC connector (RG59U) from XMT CLOCK jack on front panel to RCV CLOCK. Place CHANNEL 1 probe on center conductor. Observe a clock signal shape shown in figure.




Adjust R32 until Positive Level = /1.0/V. Adjust R34 until Negative Level = /1.0/V. Readjust if necessary.

Insert other BNC connector (d) from XMT DATA jack on front panel to RCV DATA. Place CHANNEL 2 probe on center conductor. Observe a data shape of similar levels to the XMT CLOCK shape.

Adjust R31 until Positive Level = /1.0/V. Adjust R33 until Negative Level = /1.0/V. Readjust if necessary.

5.5 **DSX Monitor Option**

Remove Monitor option from main frame. Do not disconnect 14 pin connector.

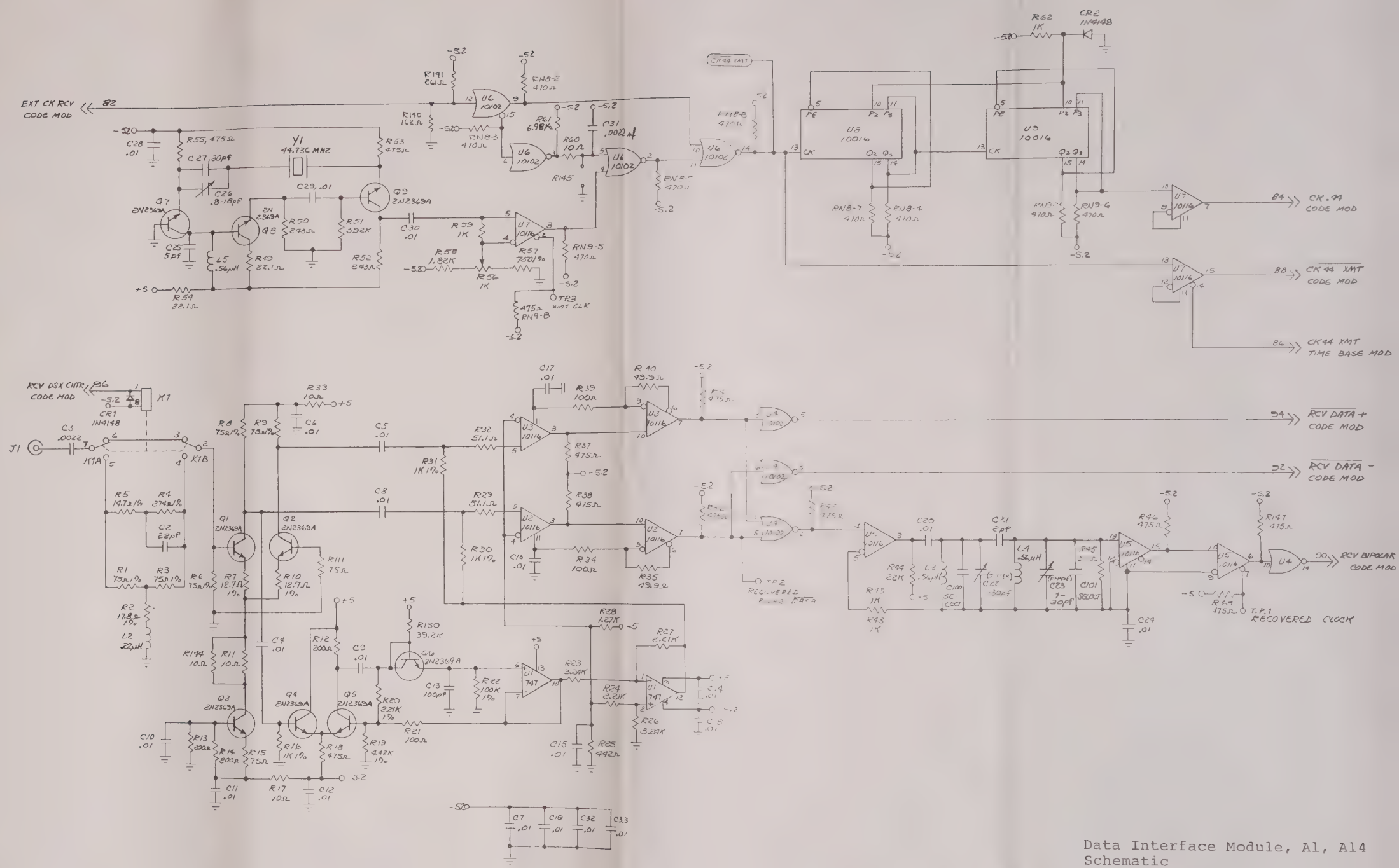
a. A15 Board
Jumper a DS3 output through a 75 ohm, 20 dB attenuator to the monitor input. Jumper the monitor output to scope input CHANNEL 1.

b. Set Front Panel switches at DSX, RANDOM. Note a DSX pattern on the scope screen at approximately 700 mV peak.

c. Adjust Trimpot R15 until the signal just becomes attenuated from its peak.

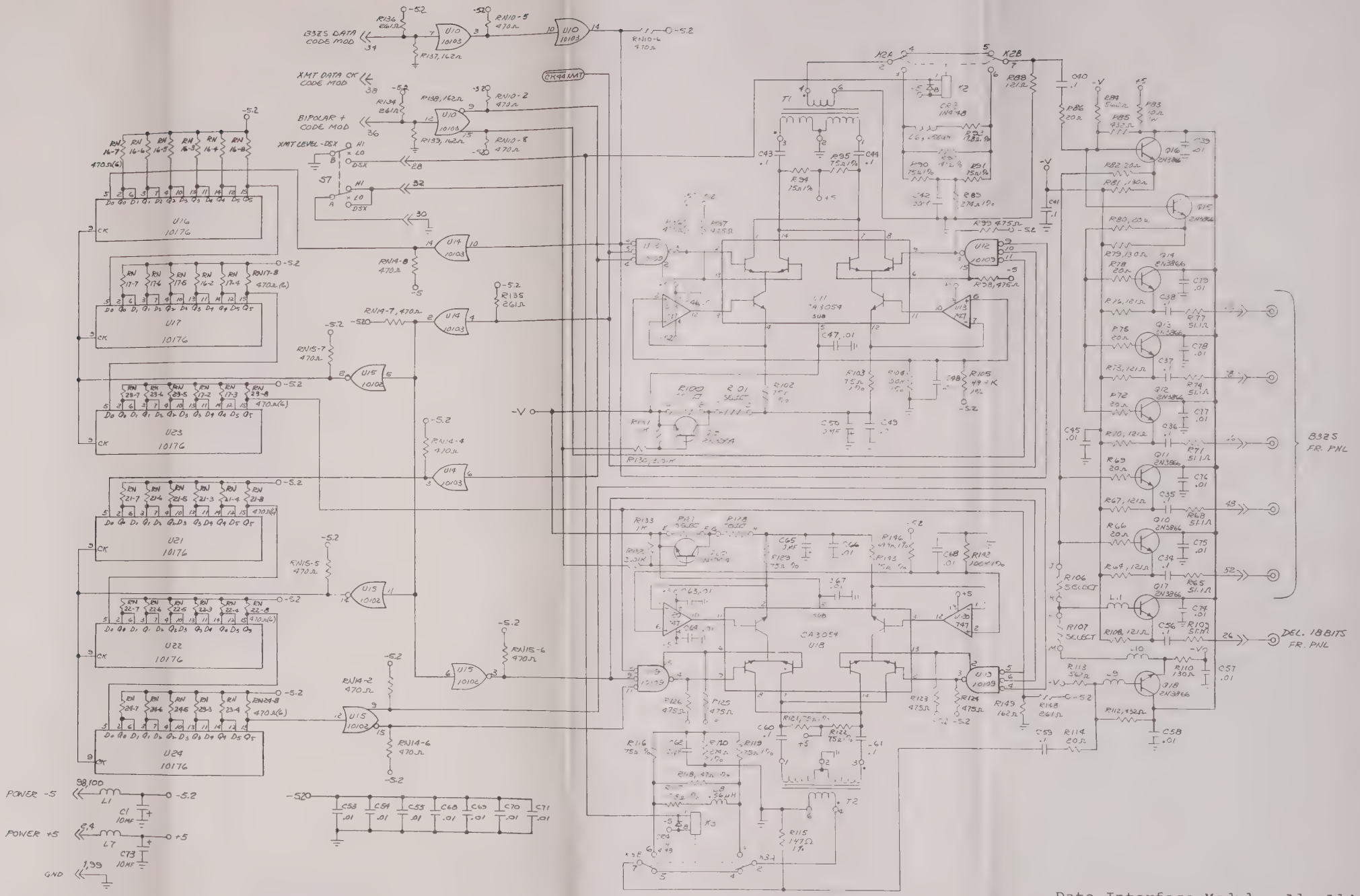
# 6.0 SCHEMATICS AND DIAGRAMS


| | | |
|---|---|---|
| FIGURE 1: | Data Interface Module Schematic, A1, A14 | 02-2751-1010/E |
| FIGURE 2: | Data Interface Module Assembly, A1, A14 | 02-2751-2012/H |
| FIGURE 3: | Code Module Schematic, A2 | 02-2751-1020/C |
| FIGURE 4: | Code Module Assembly, A2 | 02-2751-2020/C |
| FIGURE 5: | Frame & Data Module Schematic, A3 | 02-2751-1030/D |
| FIGURE 6: | Frame & Data Module Assembly, A3 | 02-2751-2030/B |
| FIGURE 7: | Sync Module Schematic, A4 | 02-2752-1530/B |
| FIGURE 8: | Sync Module Assembly, A4 | 02-2752-2530/C |
| FIGURE 9: | Timebase Module Schematic, A5 | 02-2752-1500/B |
| FIGURE 10: | Timebase Module Assembly, A5 | 02-2752-2500/F |
| FIGURE 11: | Interconnect Module Schematic, A6 | 02-2752-1540/B |
| FIGURE 12: | Interconnect Module Assembly, A6 | 02-2752-2540/E |
| FIGURE 13: | Timer Schematic, A7 | 02-2752-1520/D |
| FIGURE 14: | Timer Assembly, A7 | 02-2752-2520/C |
| FIGURE 15: | Display Module Schematic, A8 | 02-2752-1510/B |
| FIGURE 16: | Display Module Assembly, A8 | 02-2752-2510/F |
| FIGURE 17: | Power Supply Schematic, A9, A13, A16 | 02-2752-1180/C |
| FIGURE 18: | Power Supply Assembly, A9, A13 | 02-2751-2180/D |
| FIGURE 19: | NRZ Option 1 P.C. Board Schematic, A10 | 02-2753-1220/A |
| FIGURE 20: | NRZ Option 1 P.C. Board Assembly, A10 | 02-2753-2220/A |
| FIGURE 21: | NRZ Option 2 P.C. Board Schematic, A11 | 02-2753-1230/A |
| FIGURE 22: | NRZ Option 2 P.C. Board Assembly, A11 | 02-2753-2230/A |
| FIGURE 23: | 5-7V Regulator Board Schematic, A12 | 02-2751-1290/B |
| FIGURE 24: | 5-7V Regulator Board Assembly, A12 | 02-2751-2290/F |
| FIGURE 25: | DSX Monitor Option Schematic, A15 | 02-2753-1310/A |
| FIGURE 26: | DSX Monitor Option Assembly, A15 | 02-2753-2310/B |
| FIGURE 27: | Linear Power Supply Assembly, A16 | 02-2752-2550/C |



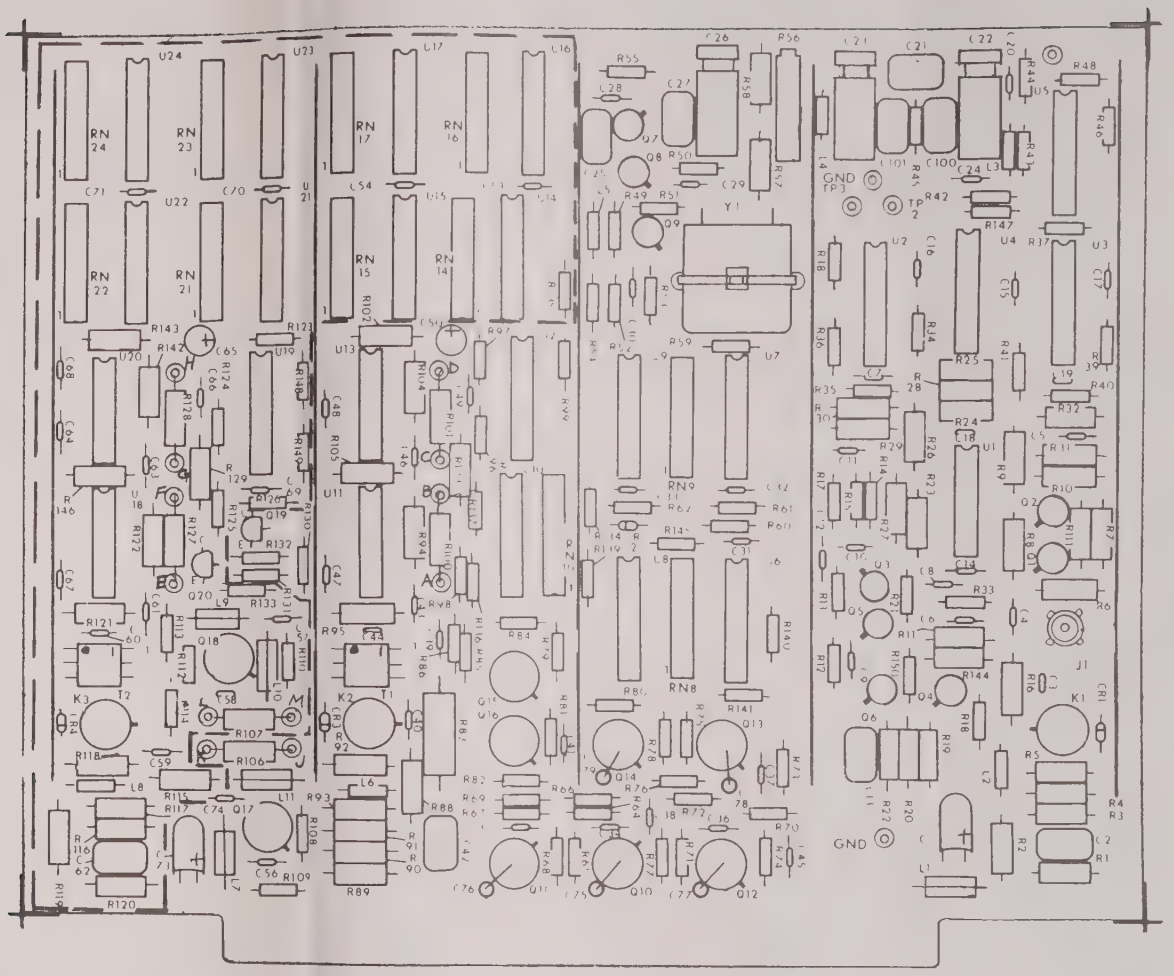

Data Interface Module, A1, A14
Schematic
02-2751-1010

**FIGURE 1** (Sheet 1)



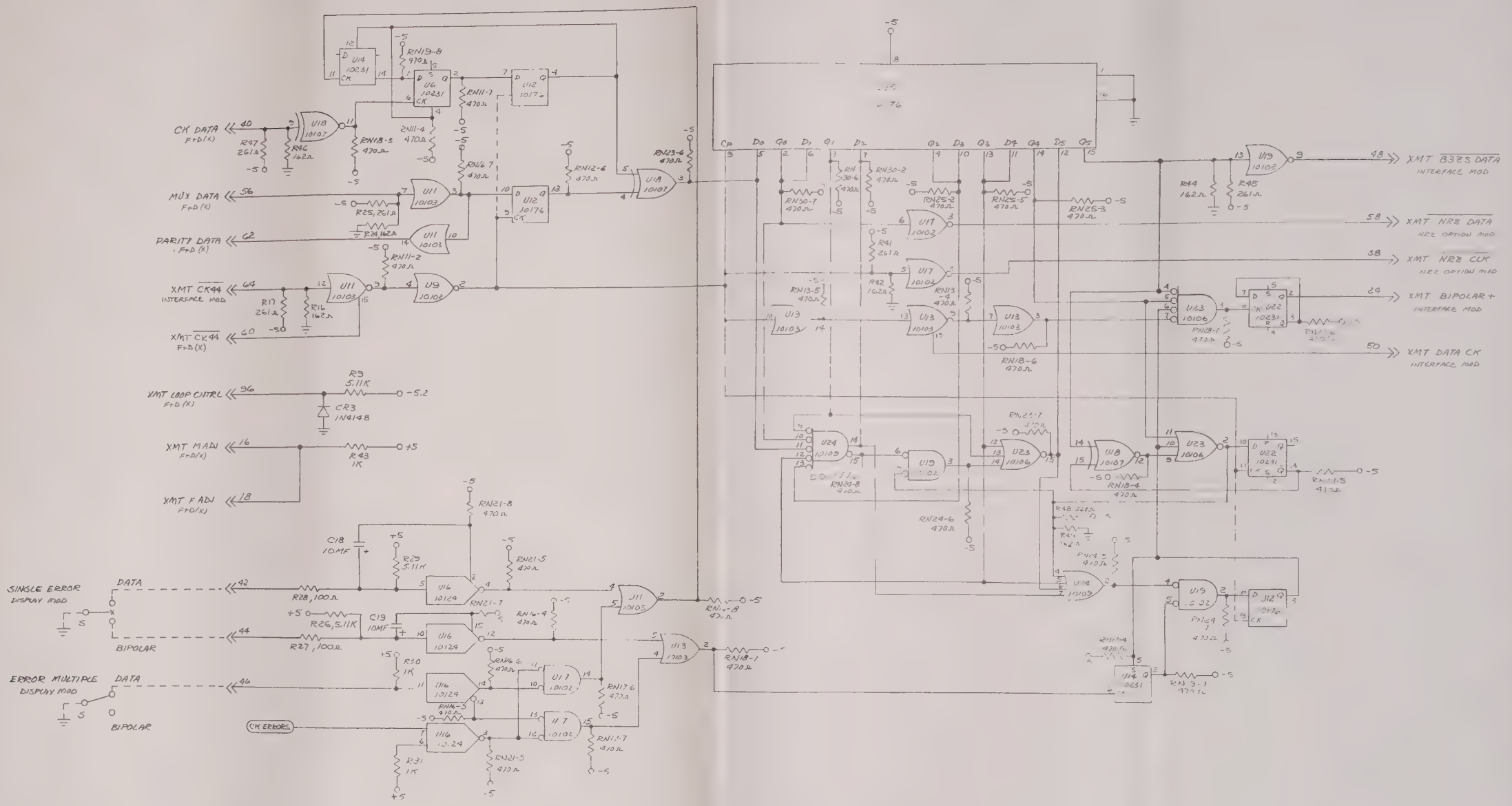

Data Interface Module, A1, A14
Schematic
02-2750-1010

**FIGURE 1** (Sheet 2)



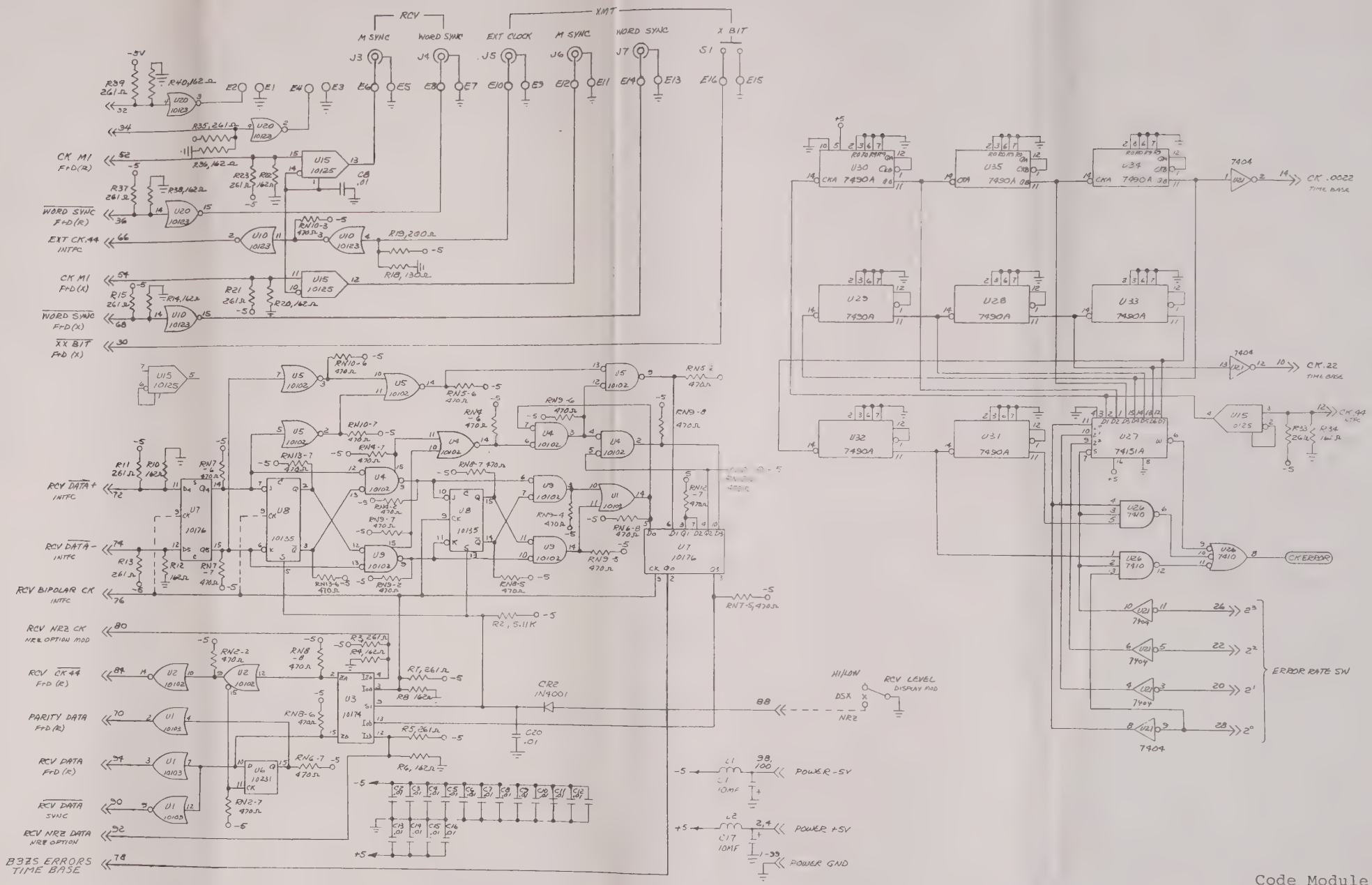
Data Interface Module, A1, A14
Assembly
02-2751-2012

**FIGURE 2**



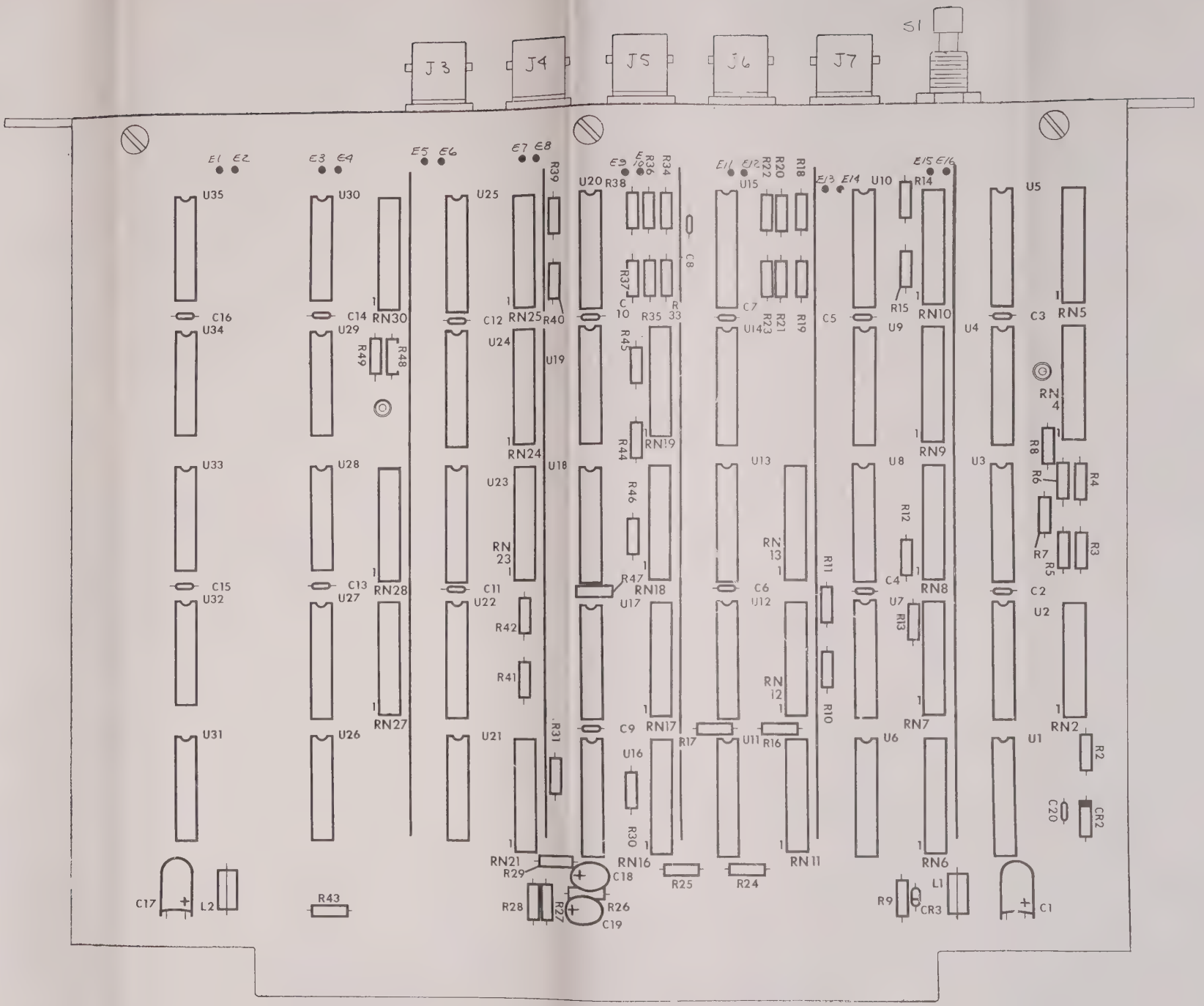

Code Module, A2
Schematic
02-2751-1020

**FIGURE 3** (Sheet 1)



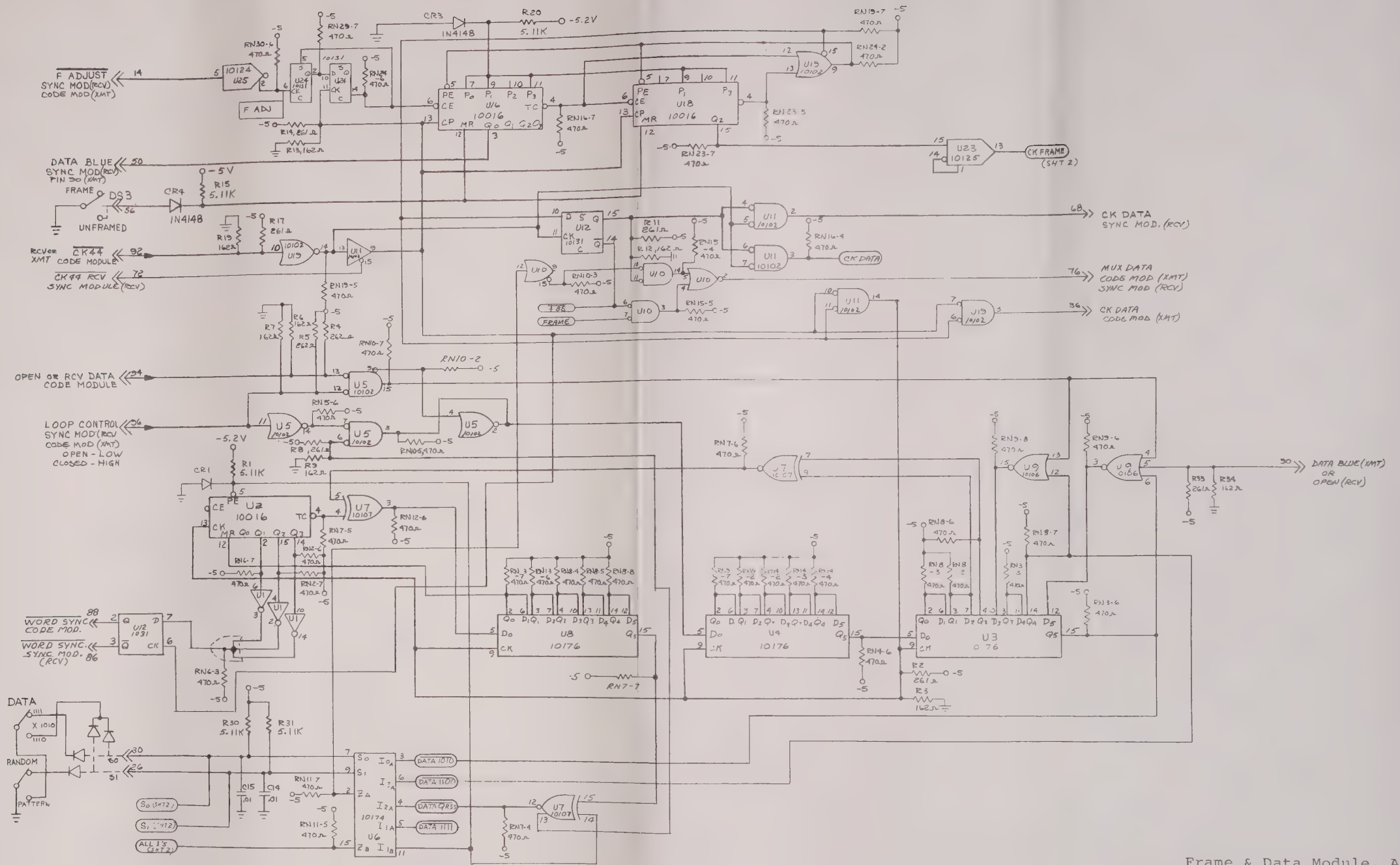

Code Module, A2
Schematic
02-2751-1020

**FIGURE 3** (Sheet 2)



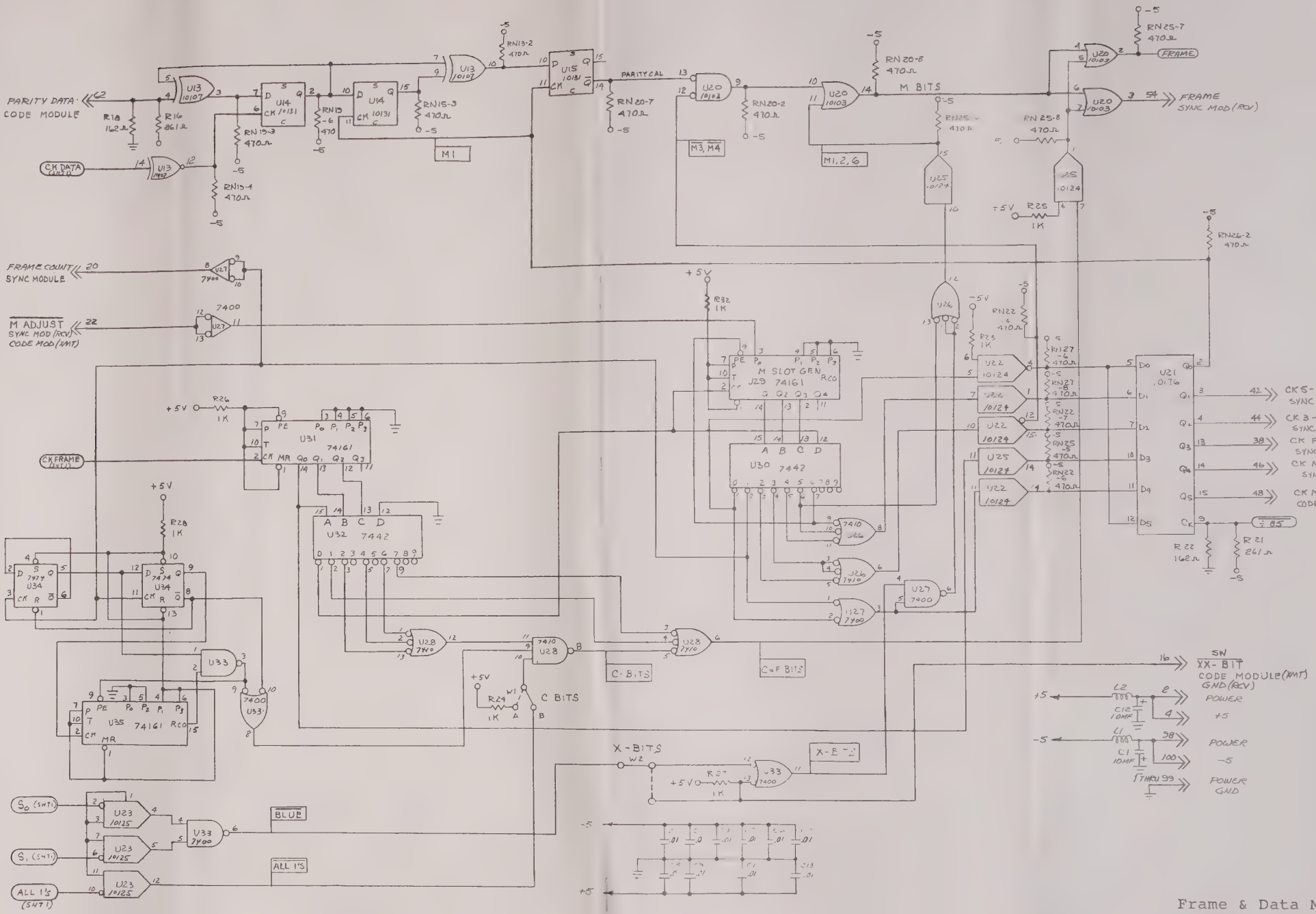

Code Module, A2
Assembly
02-2751-2020

**FIGURE 4**



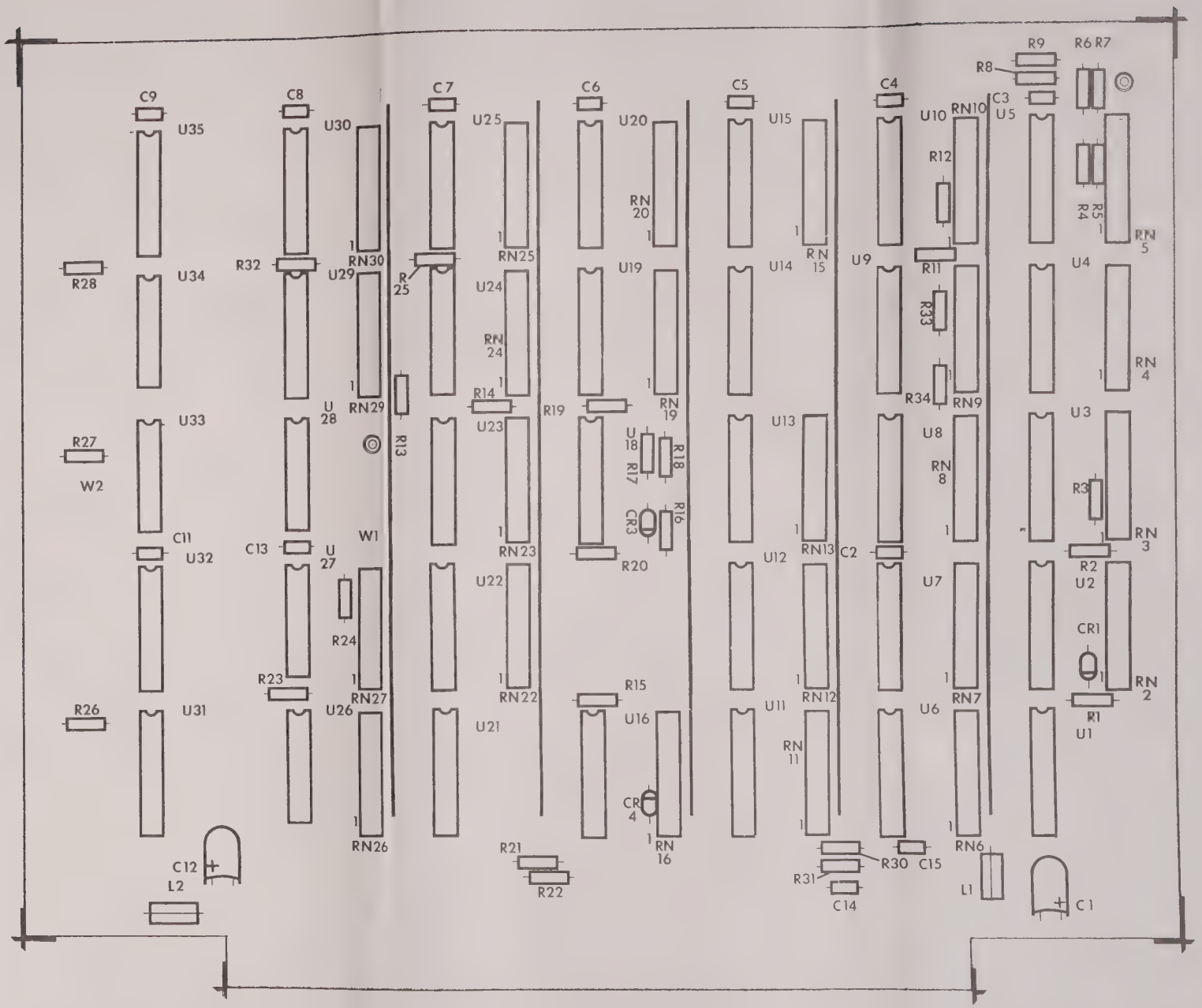

Frame & Data Module, A3
Schematic
02-2751-1030

**FIGURE 5** (Sheet 1)




Frame & Data Module, A3
Schematic
02-2751-1030

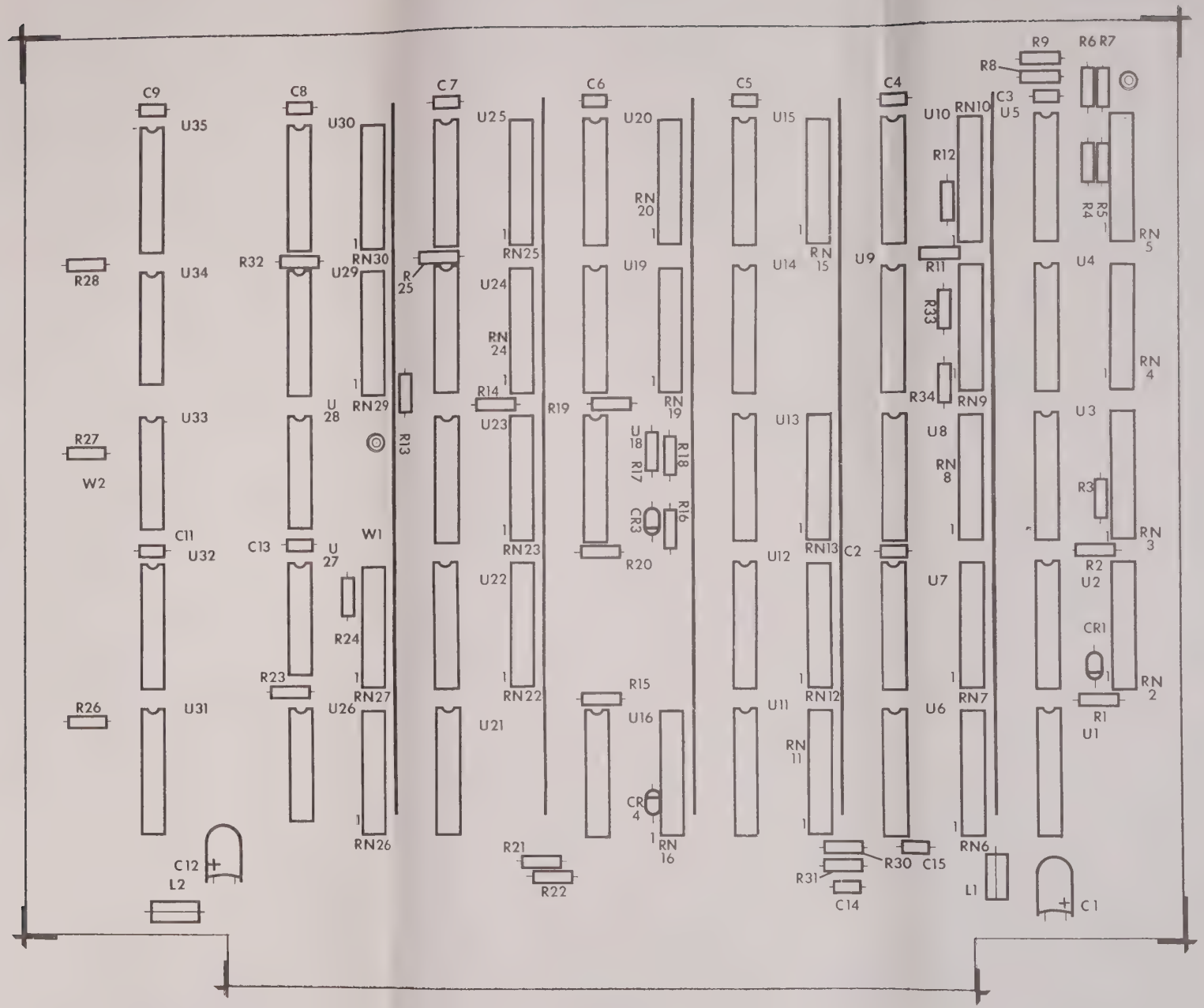
**FIGURE 5** (Sheet 2)




COMPONENT SIDE

Frame & Data Module, A3 Assembly
02-2751-2030

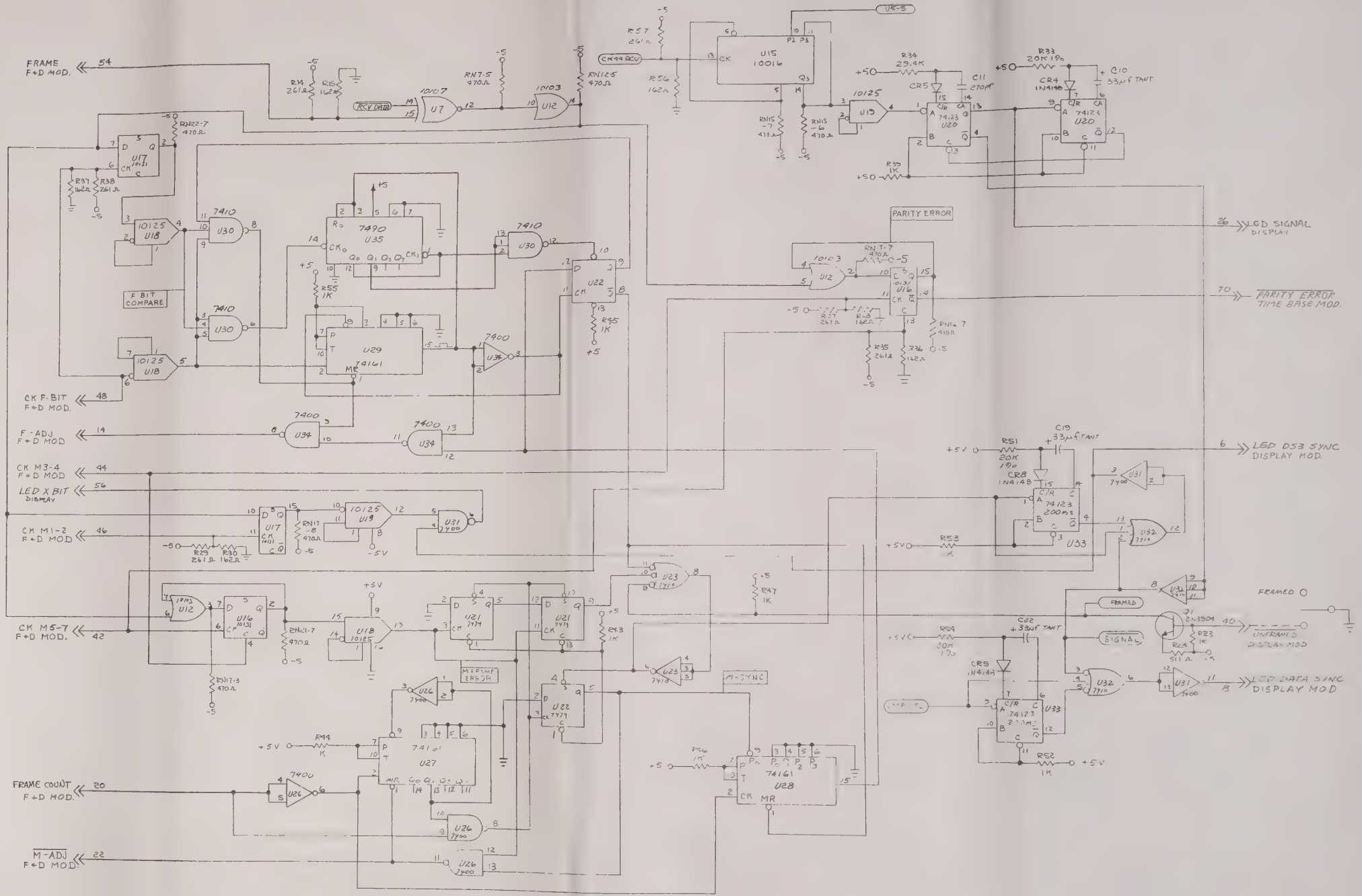
FIGURE 6




COMPONENT SIDE

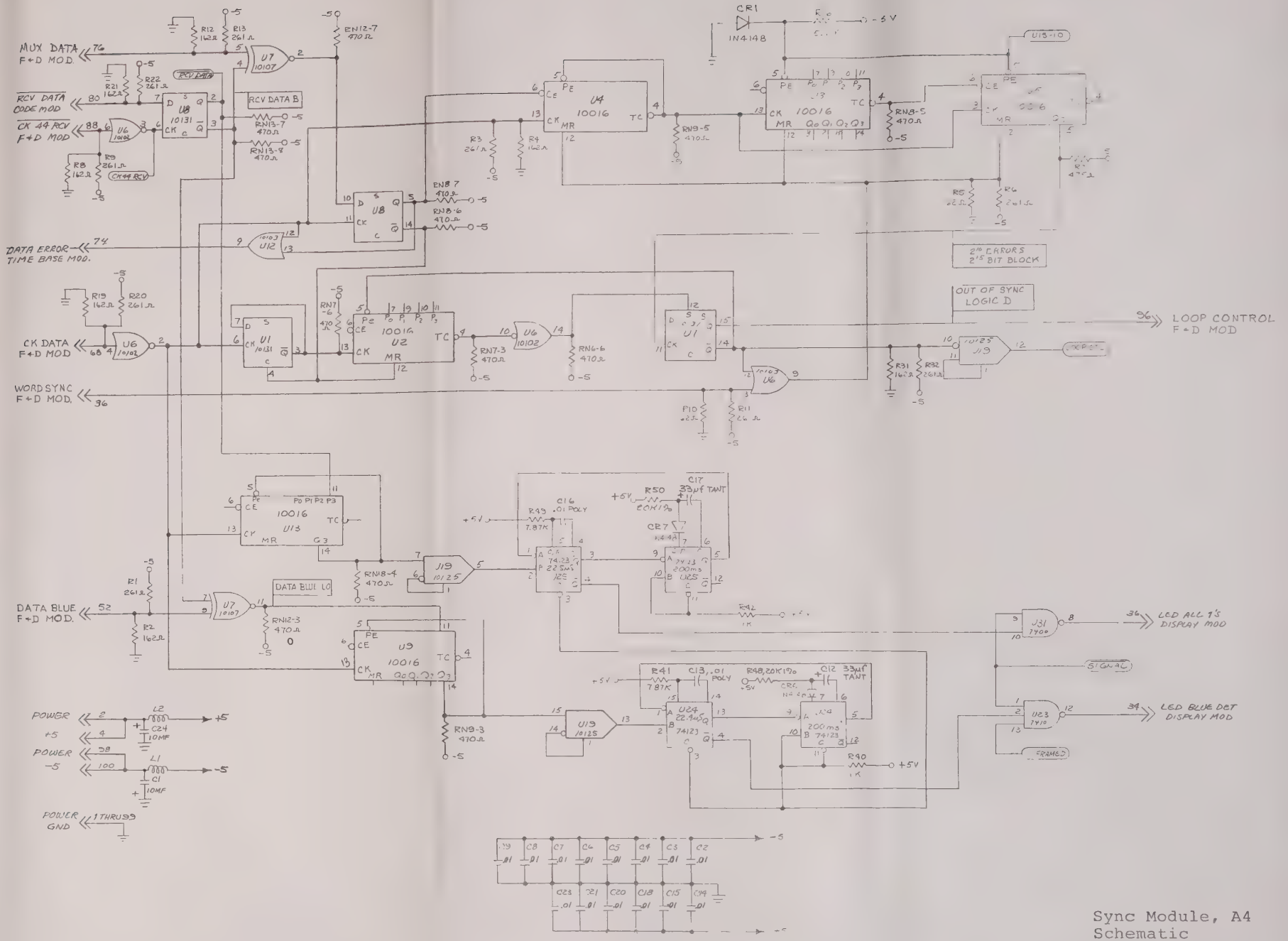
Frame & Data Module, A3 Assembly
02-2751-2030

FIGURE 6



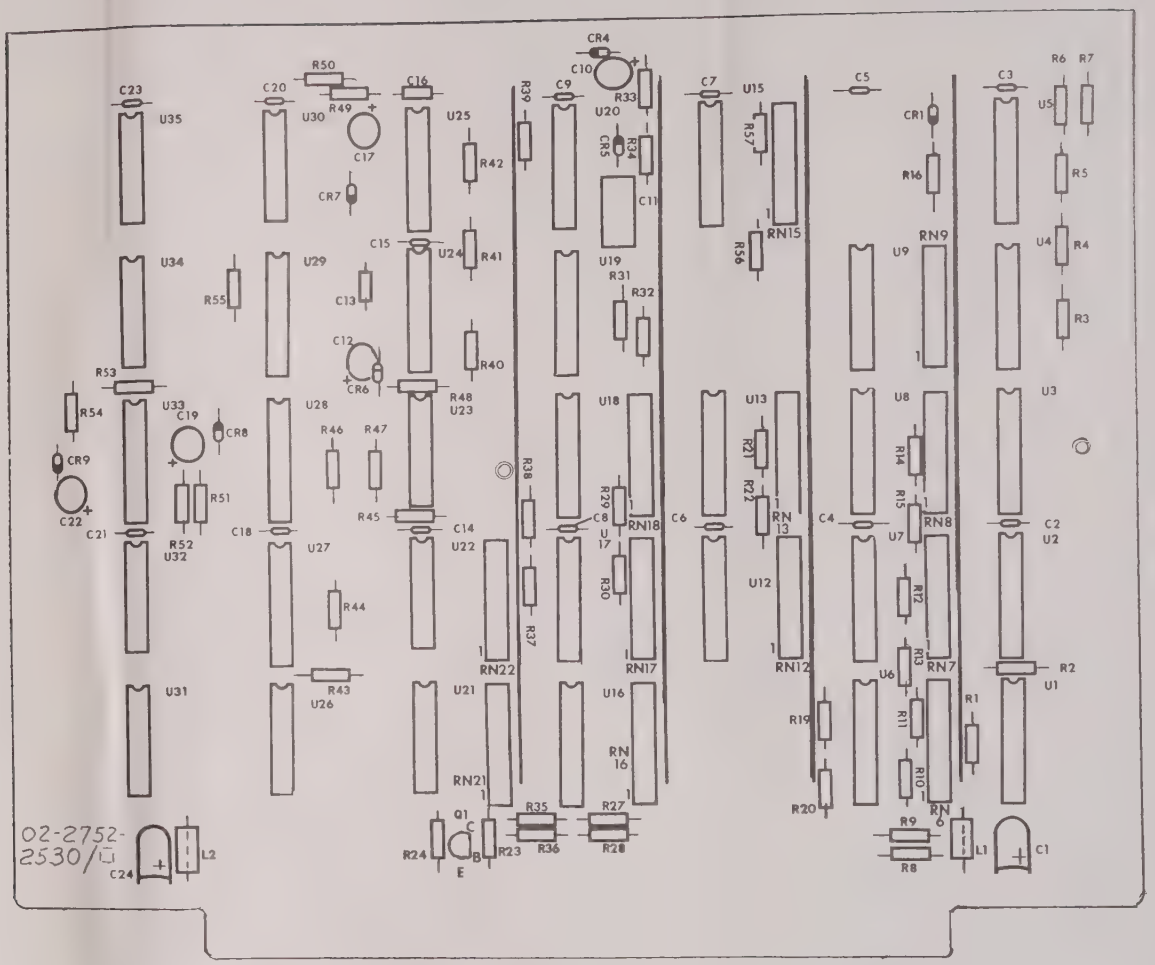

Sync Module, A4
Schematic
02-2752-1530

**FIGURE 7** (Sheet 1)



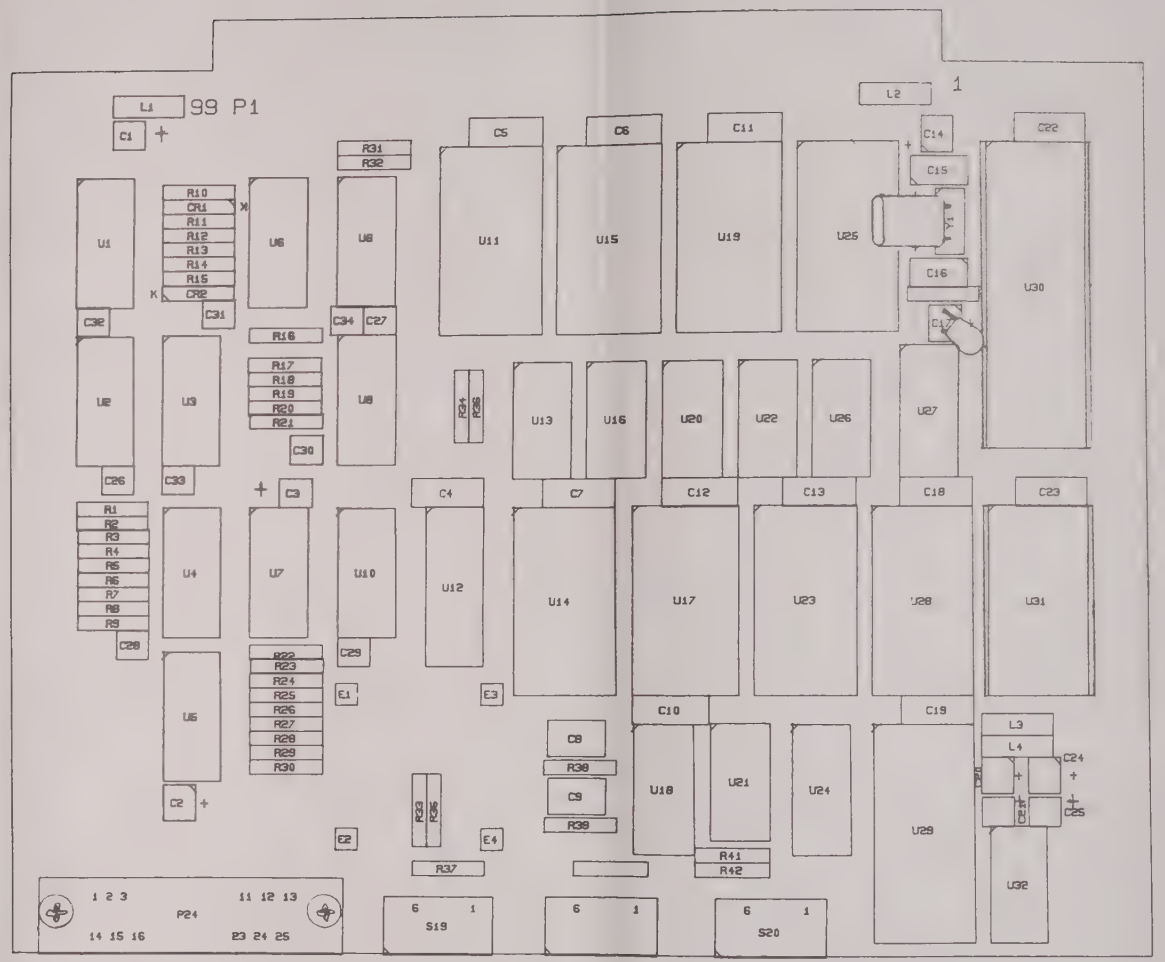

Sync Module, A4
Schematic
02-2752-1530

**FIGURE 7** (Sheet 2)



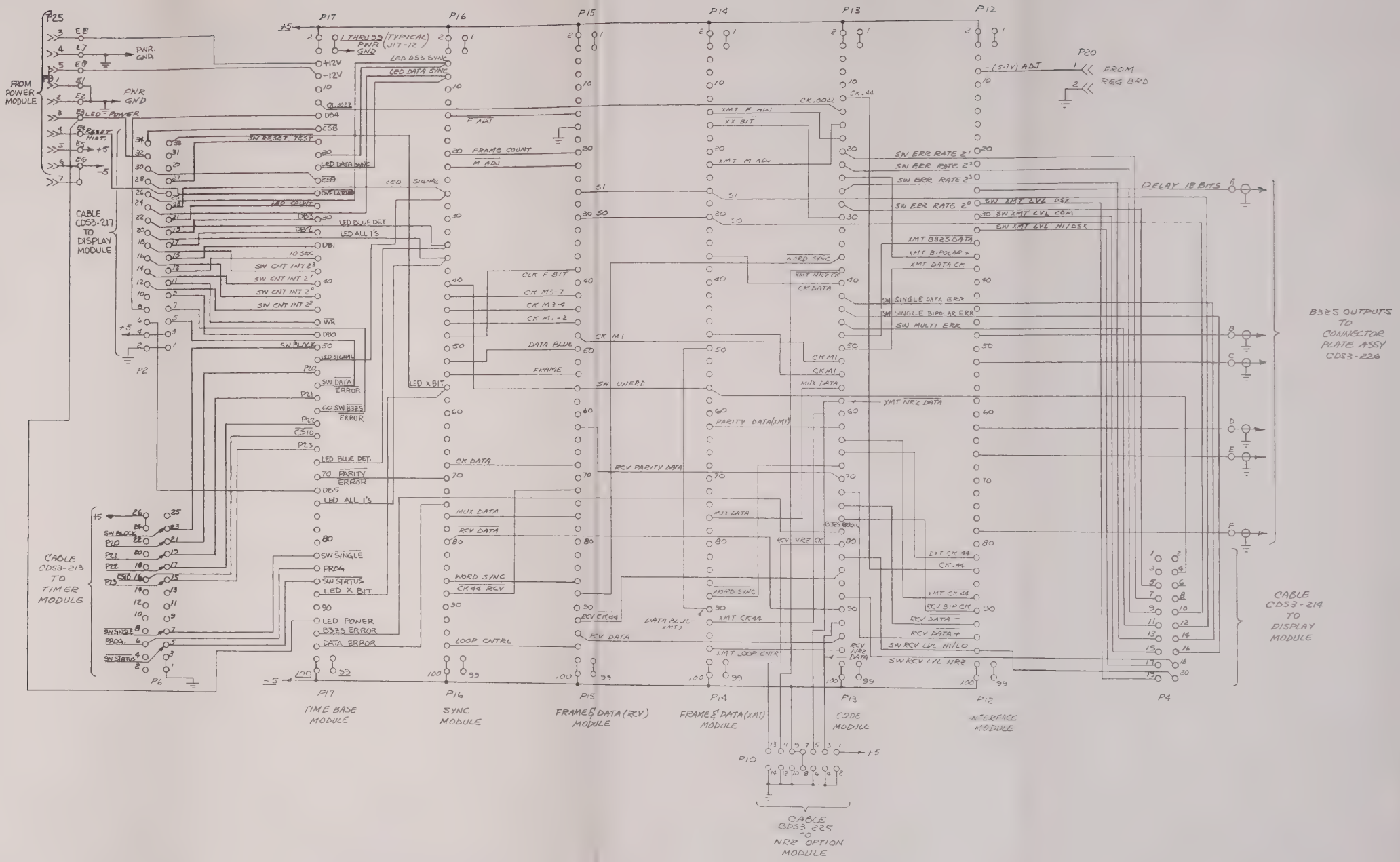

Sync Module, A4
Assembly
02-2752-2530

**FIGURE 8**



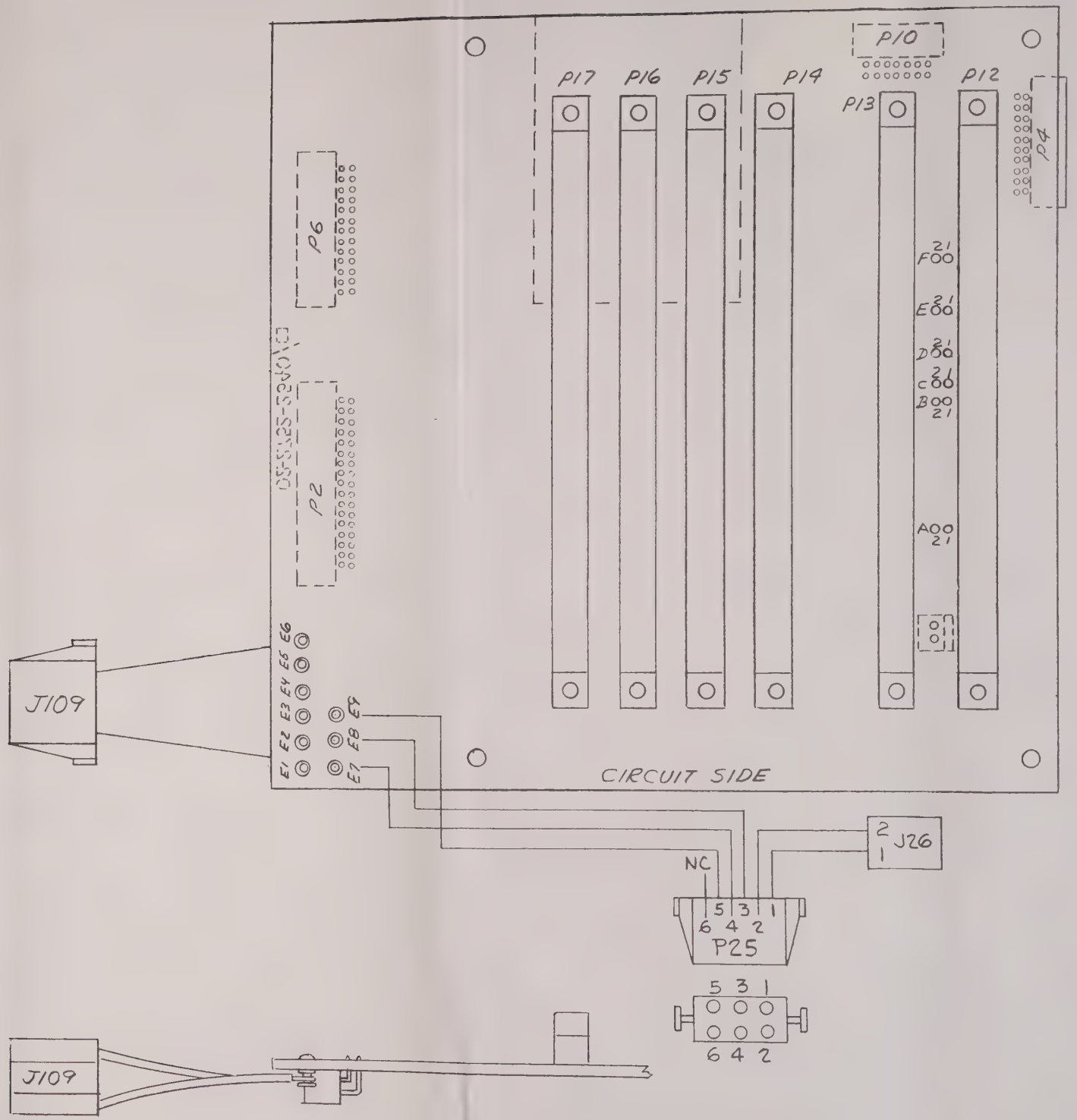

Timebase Module, A5
Assembly
02-2752-2500

**FIGURE 10**



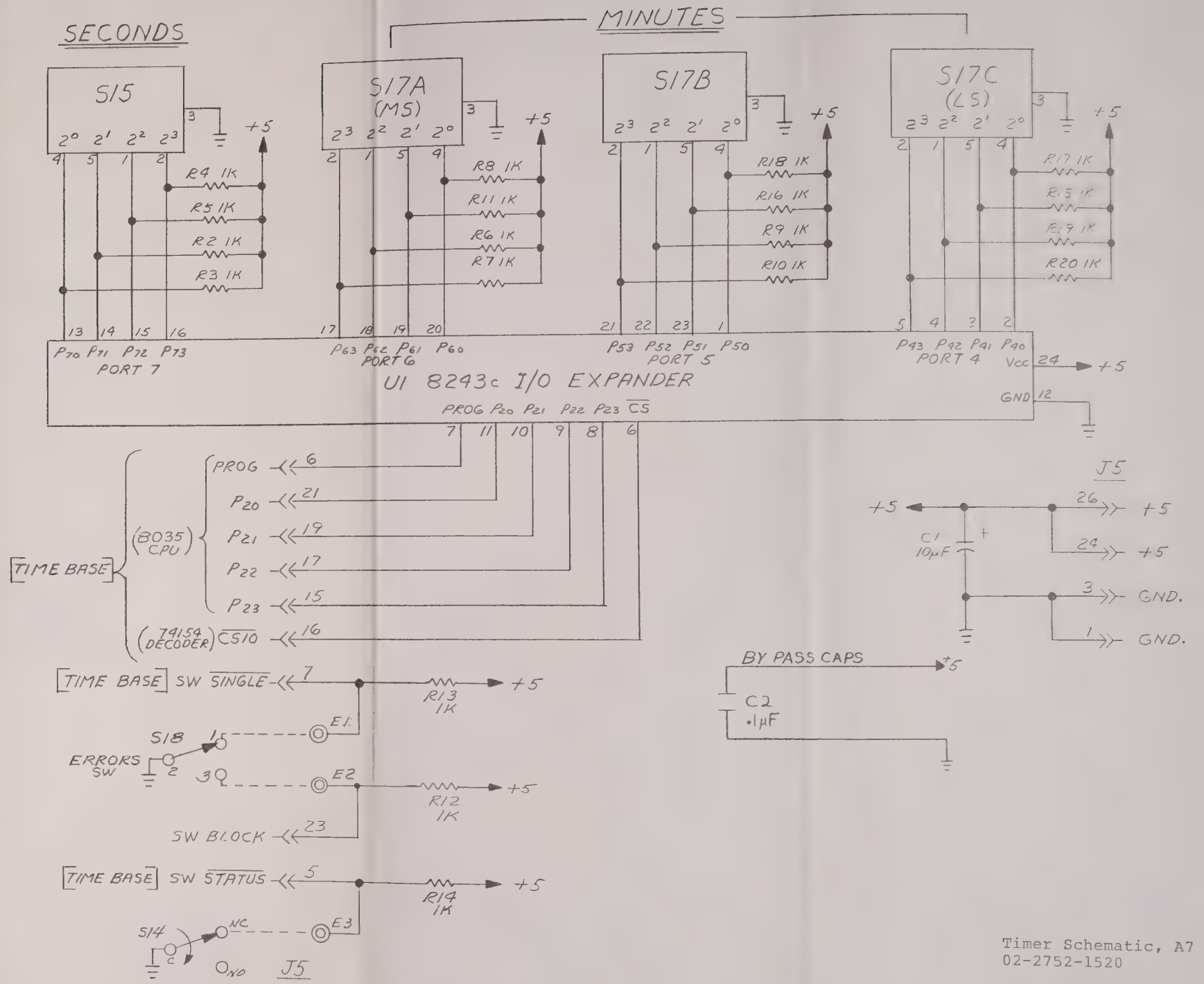

Interconnect Module, A6
Schematic
02-2752-1540

**FIGURE 11**



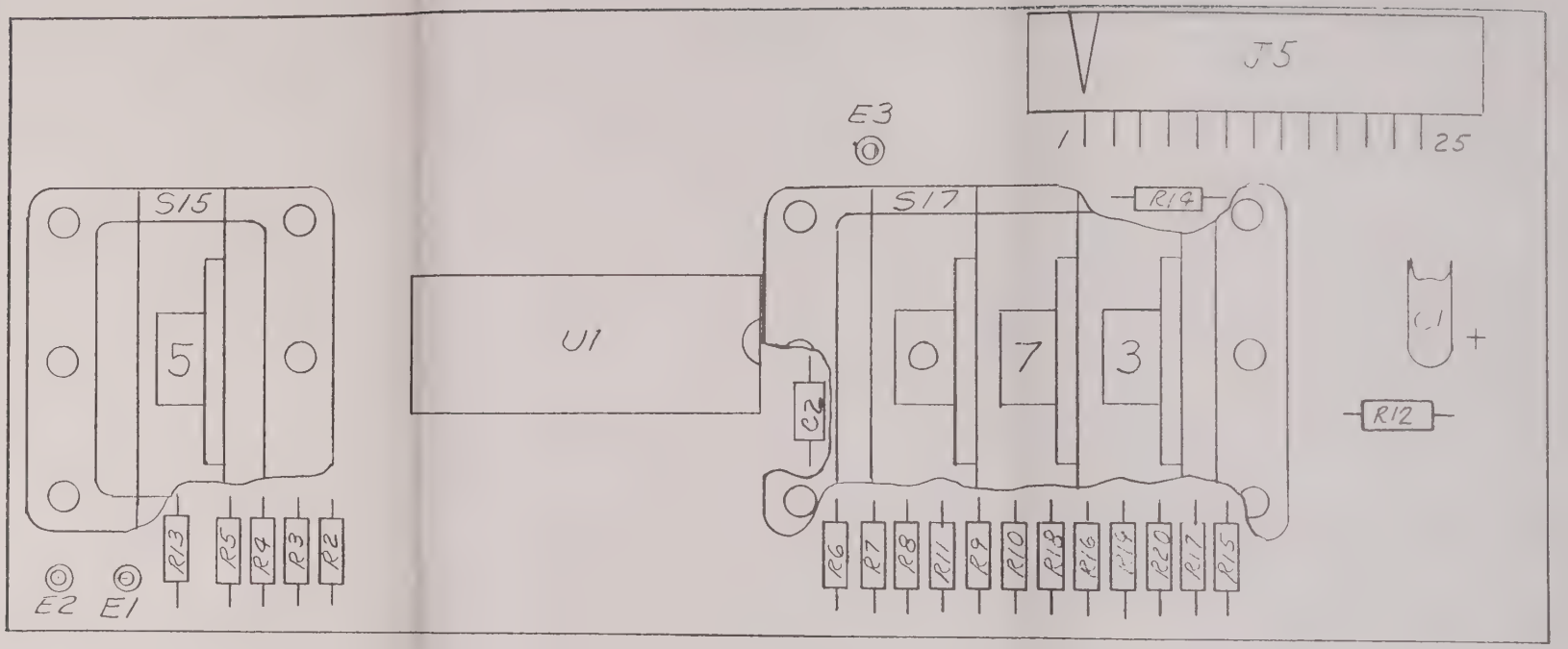

Interconnect Module, A6
Assembly
02-2752-2540

**FIGURE 12**



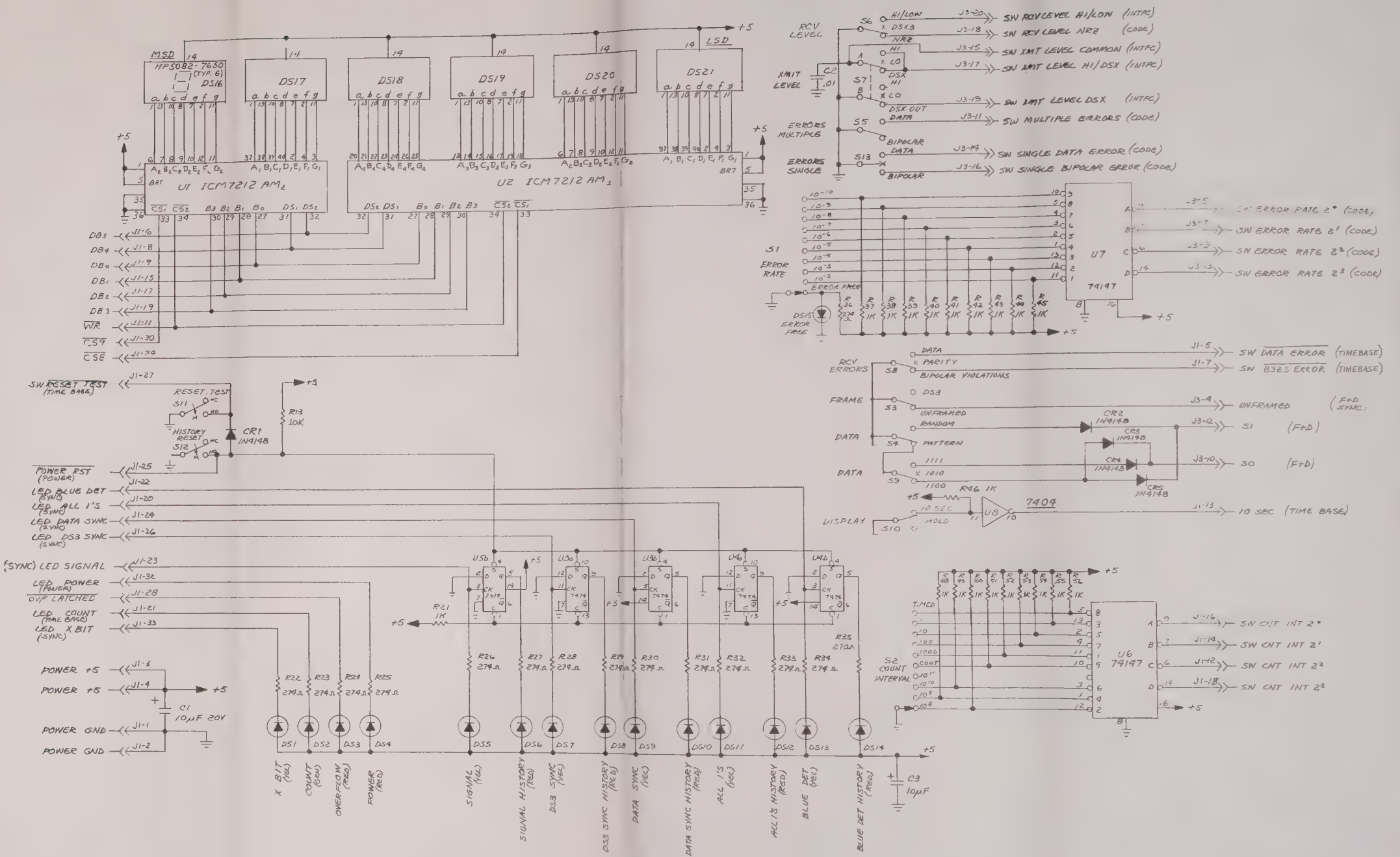

Timer Schematic, A7
02-2752-1520

**FIGURE 13**



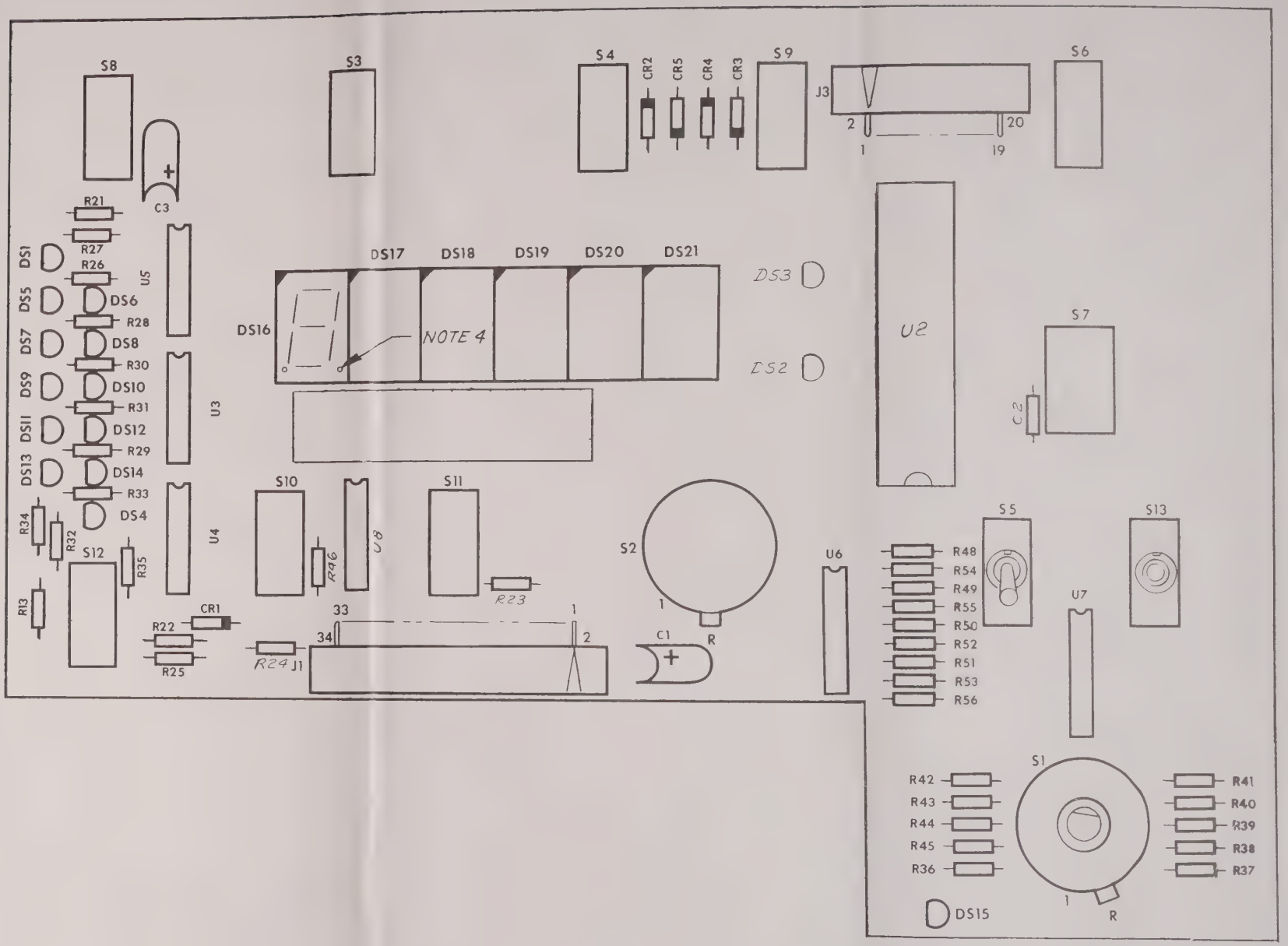

Timer Assembly, A7
02-2752-2520

**FIGURE 14**



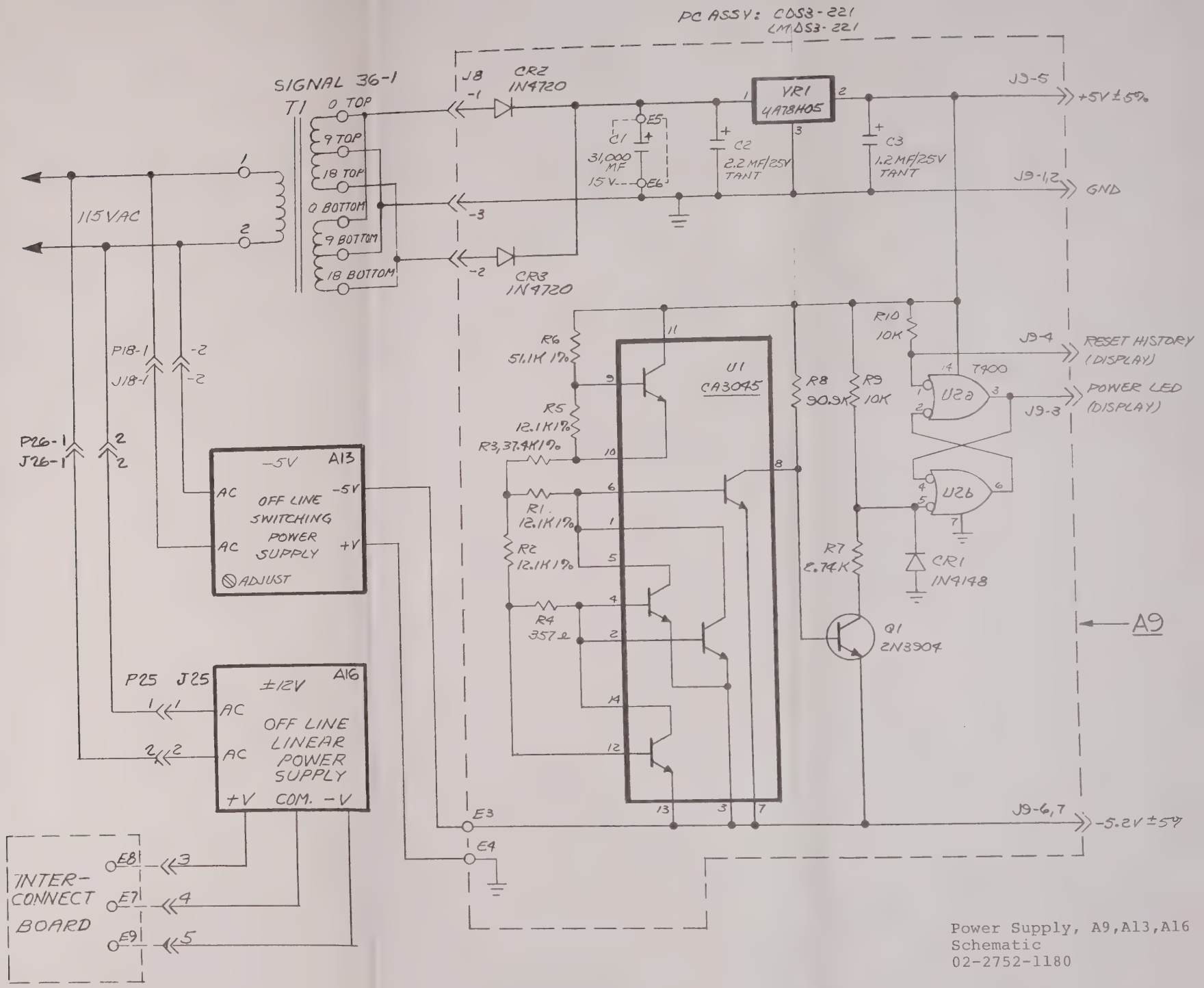

Display Module, A8
Schematic
02-2752-1510

FIGURE 15



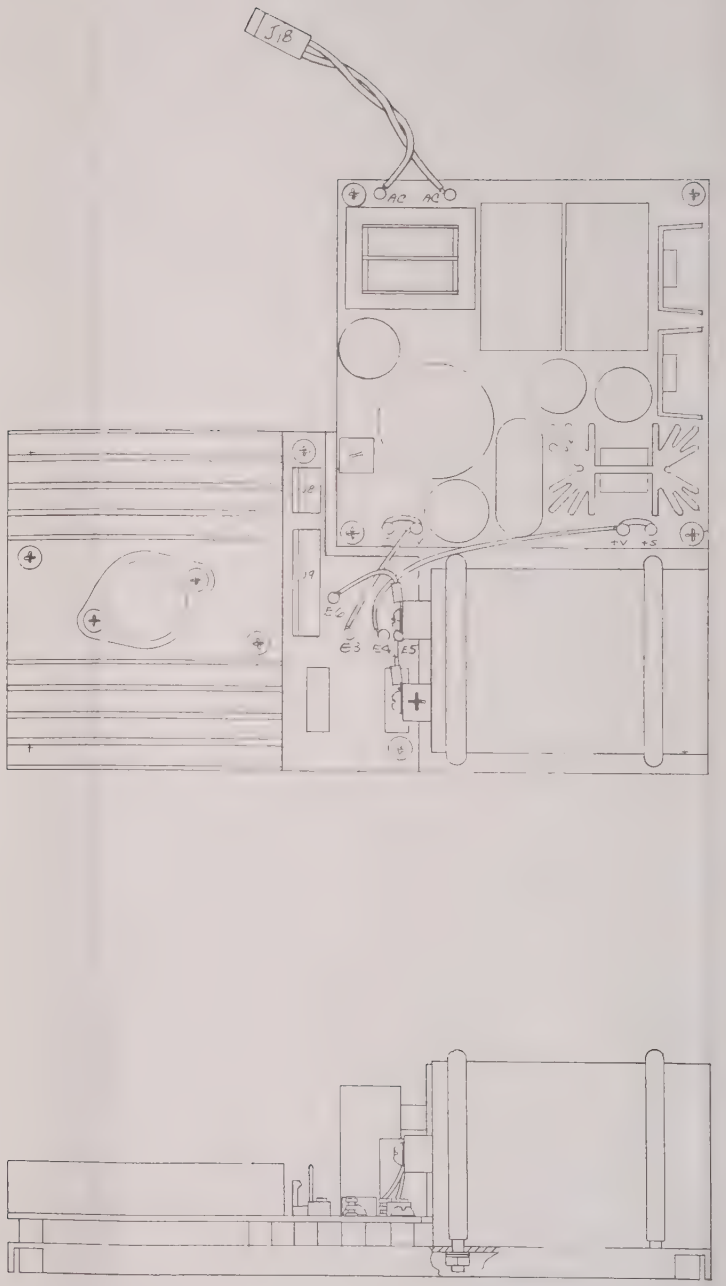

Display Module, A8
Assembly
02-2752-2510

FIGURE 16



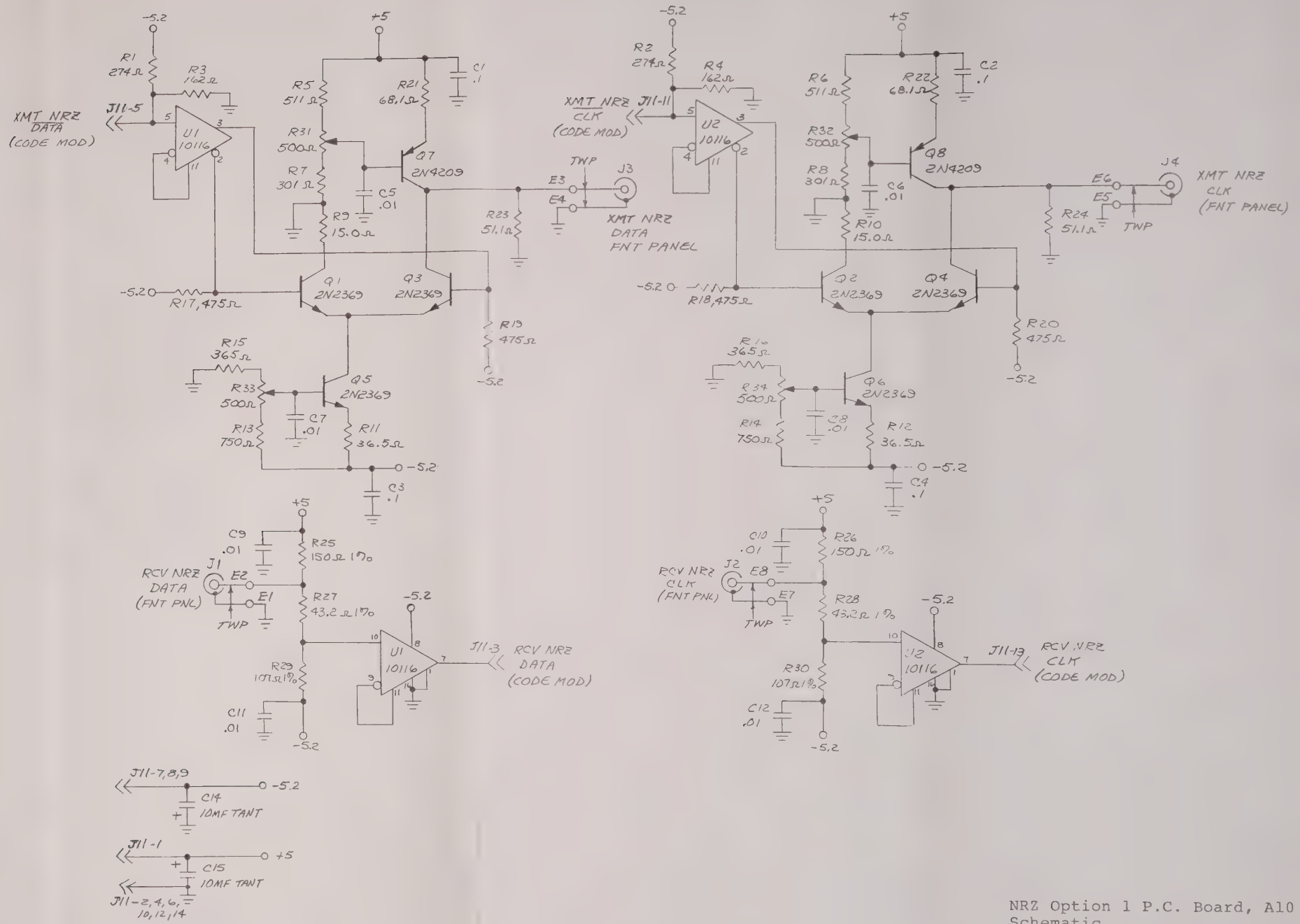

Power Supply, A9,A13,A16
Schematic
02-2752-1180

FIGURE 17



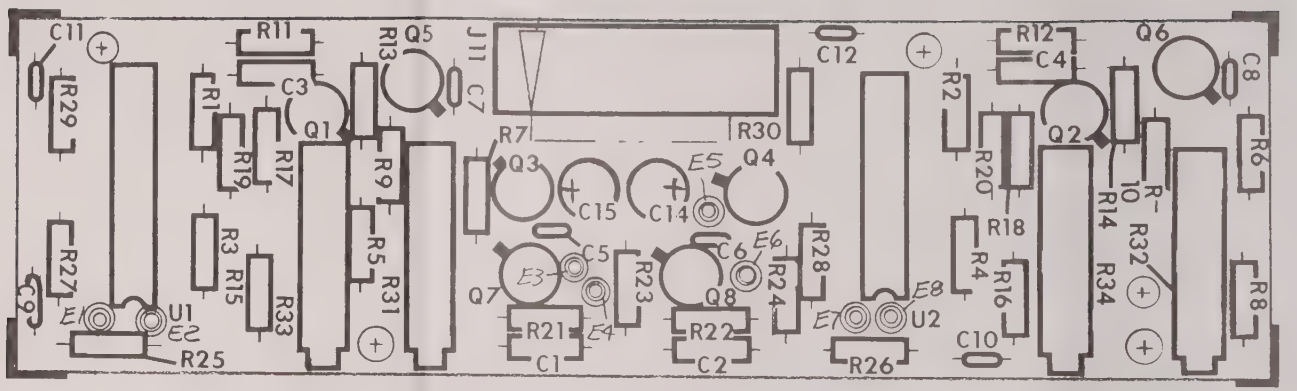

Power Supply, A9,A13
Assembly
02-2751-2180

**FIGURE 18**




NRZ Option 1 P.C. Board, A10
Schematic
02-2753-1220

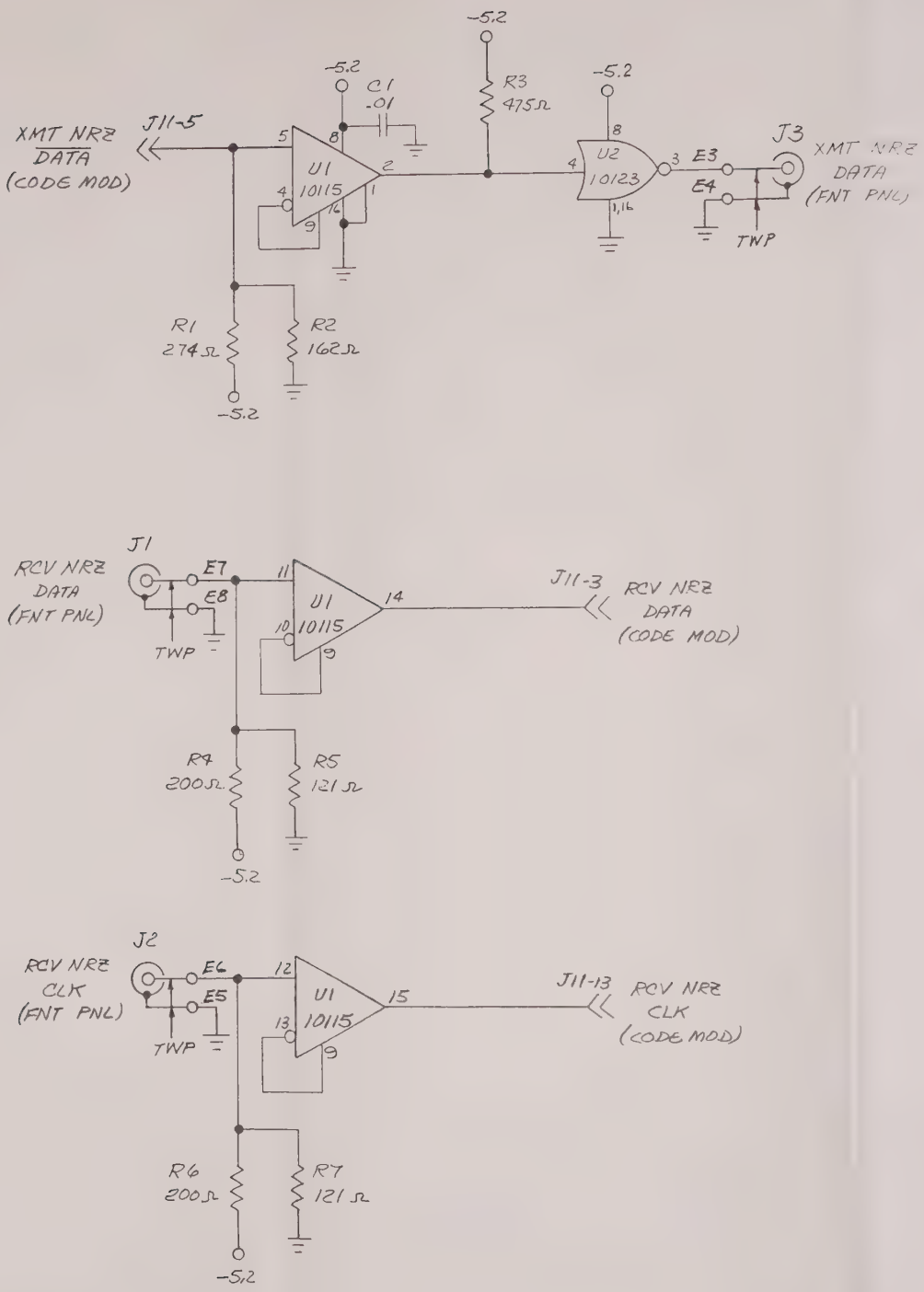
**FIGURE 19**




COMPONENT
SIDE

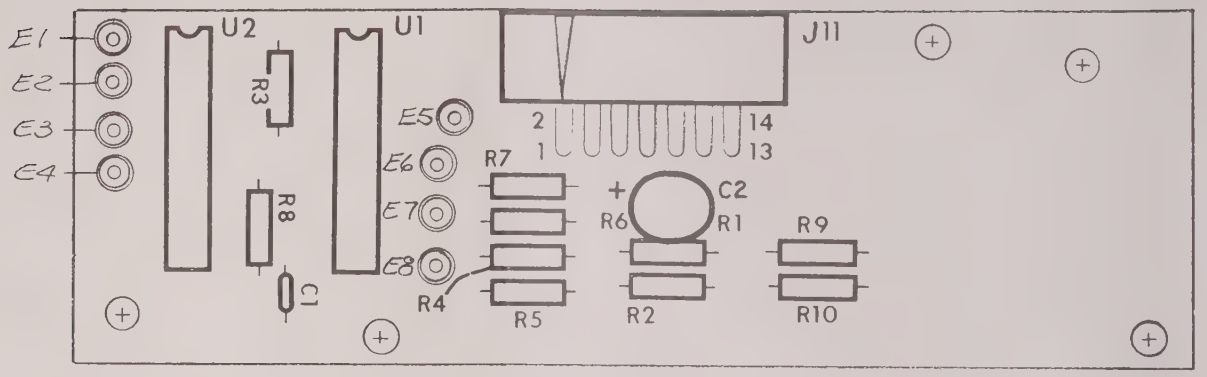
NRZ Option 1 P.C. Board, A10
Assembly
02-2753-2220

FIGURE 20




NRZ Option 2 P.C. Board, All Schematic
02-2753-1230

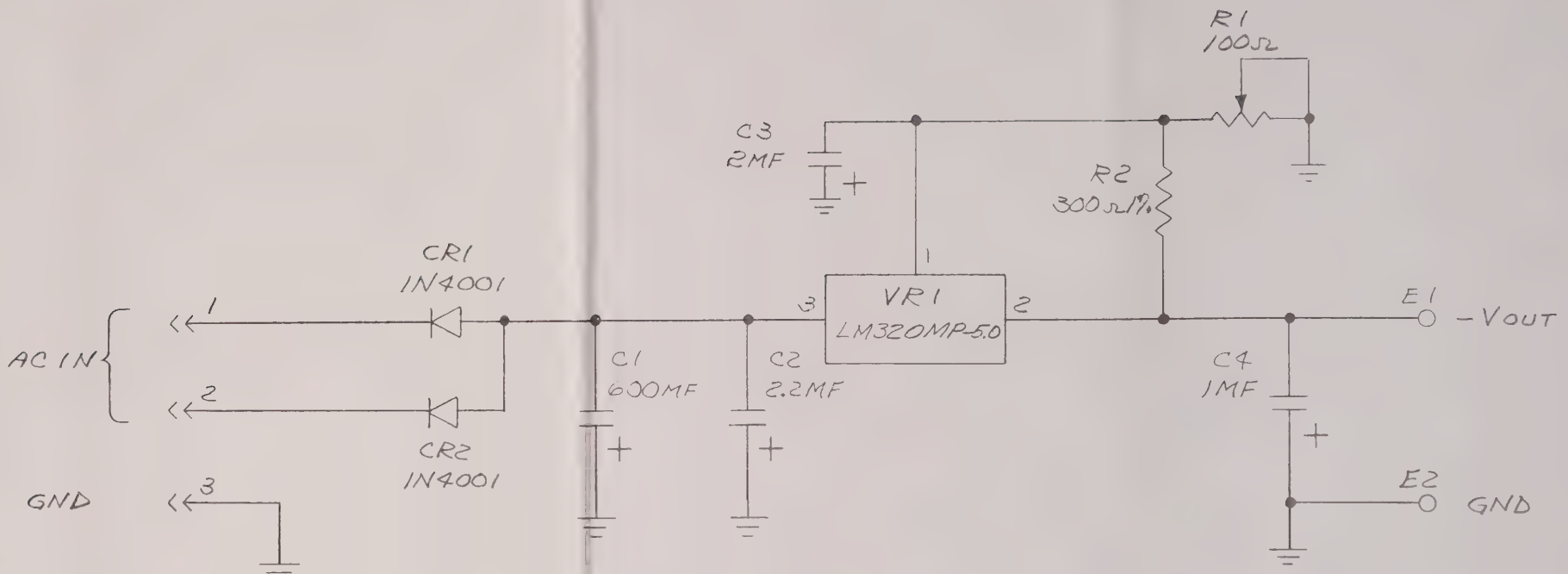
**FIGURE 21**




COMPONENT SIDE

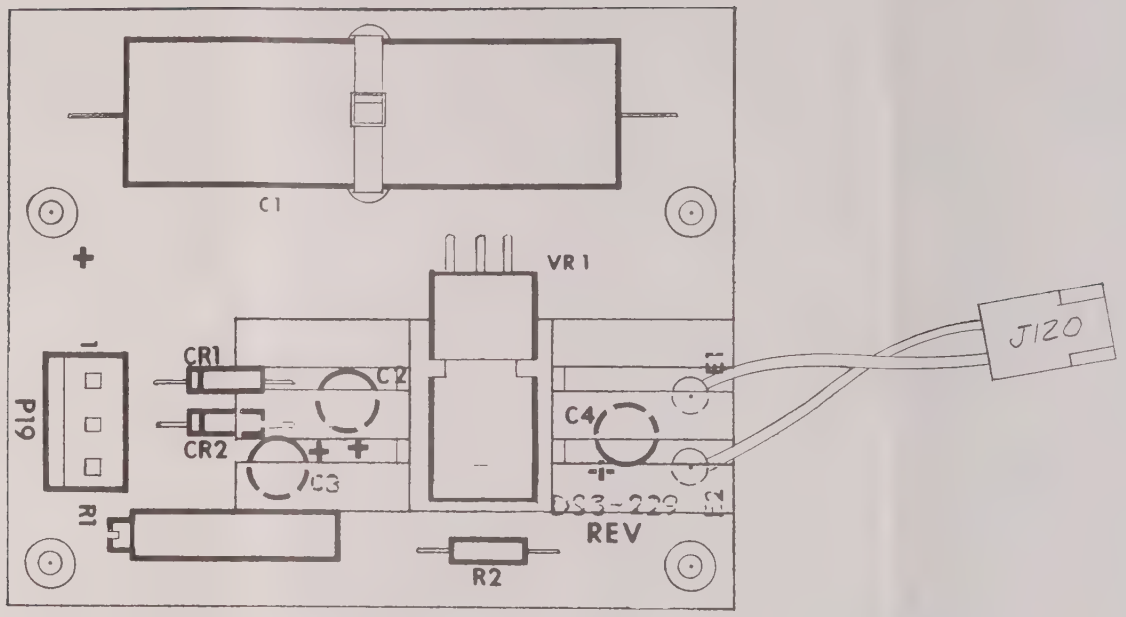
NRZ Option 2 P.C. Board, All Assembly
02-2753-2230

FIGURE 22



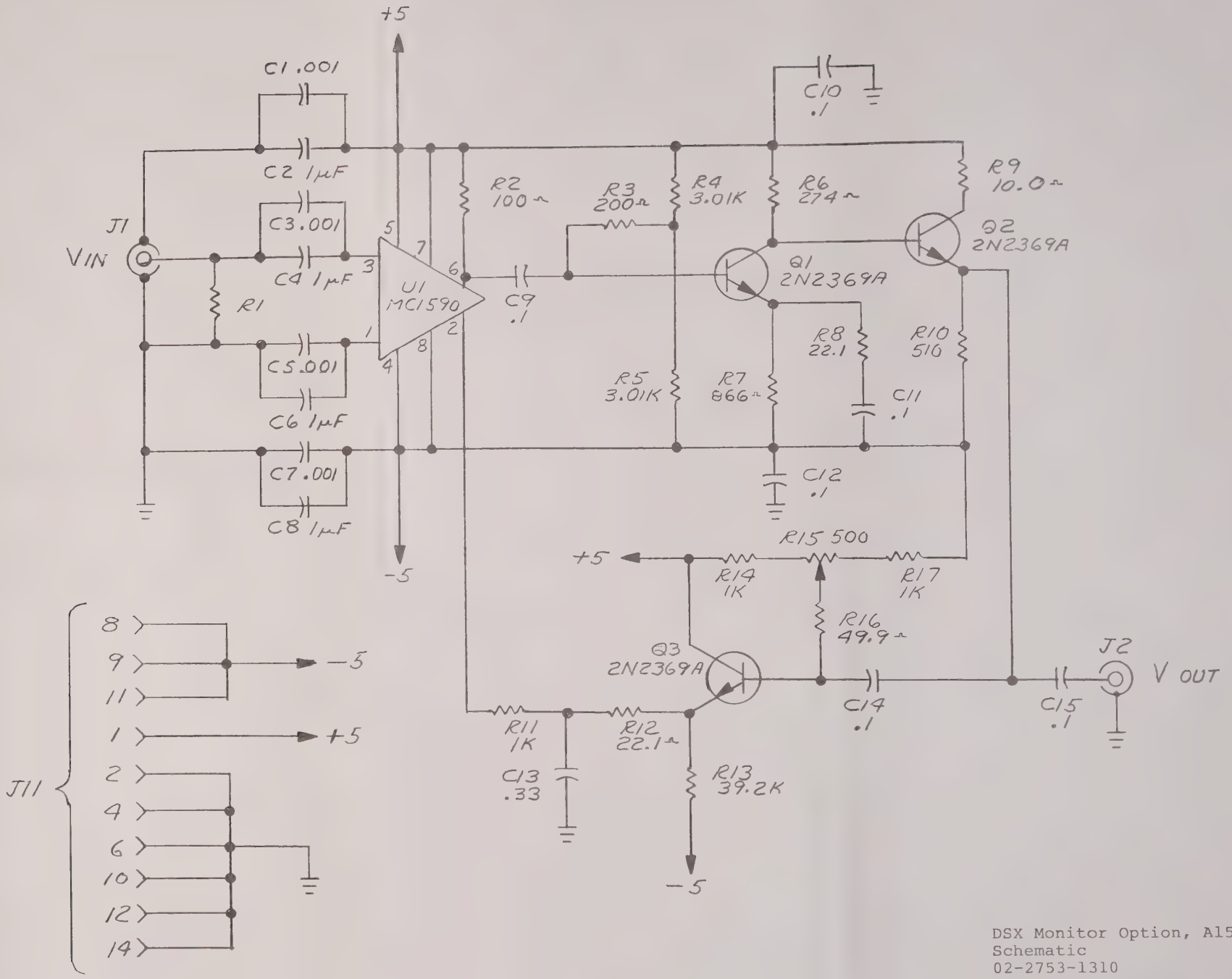

5-7V Regulator Board, A12
Schematic
02-2751-1290

**FIGURE 23**



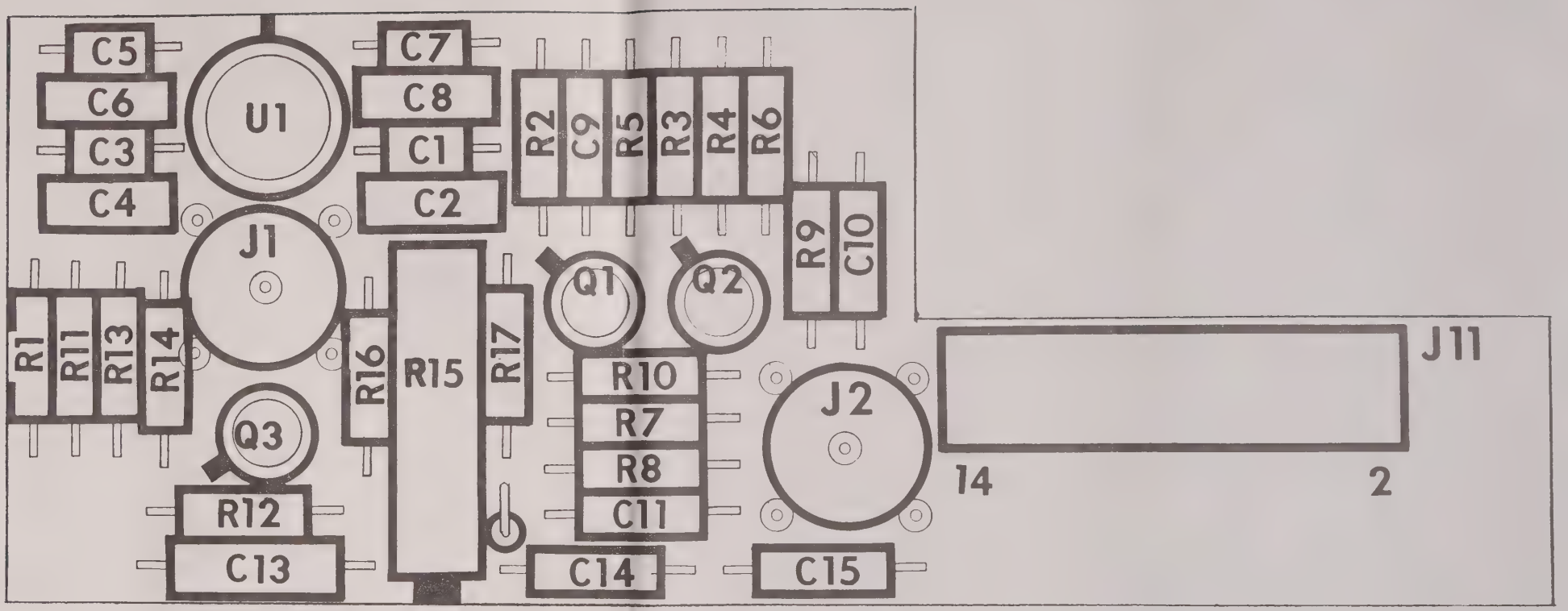

5-7V Regulator Board, A12
Assembly
02-2751-2290

FIGURE 24



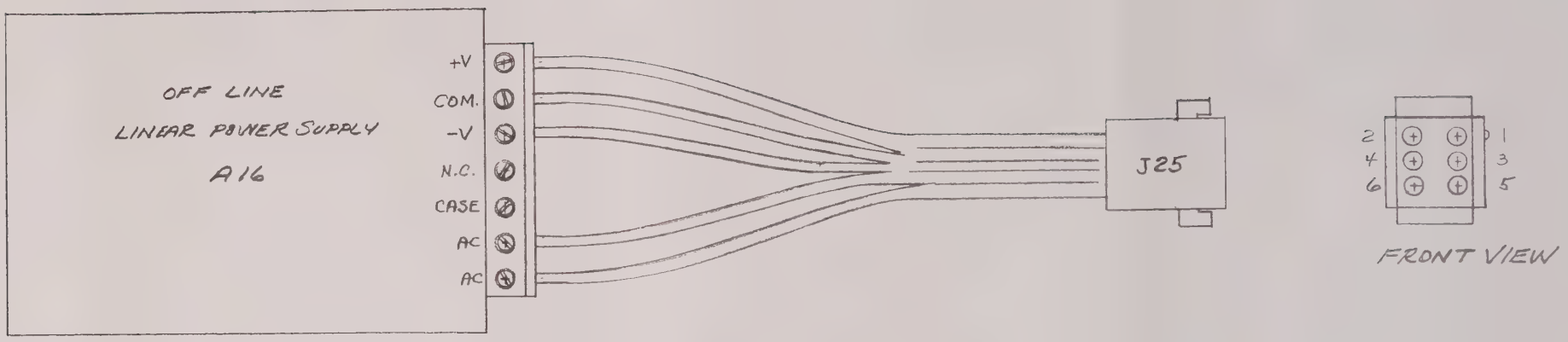

DSX Monitor Option, A15
Schematic
02-2753-1310

**FIGURE 25**




DSX Monitor Option, A15
Assembly
02-2753-2310

**FIGURE 26**




Linear Power Supply, A16
Assembly
02-2752-2550

**FIGURE 27**

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **NRZ CABLE ASSEMBLY - 02-2752-2550** | | | | |
| J25 | Connector, 6 Pin | AMP | 1-480340-0 | 34-0300-0082 |
| **CONNECTOR PLATE ASSEMBLY (358) - 02-2751-2261** | | | | |
| J21-27 | Connector, 1 Pin | Trompeter | J3WE-5 | 34-0400-0005 |
| P1 | Connector, 1 Pin | Amphenol | 27-26 | 34-0400-0004 |
| **CONNECTOR PLATE ASSEMBLY (440) - 02-2751-2262** | | | | |
| J21-27 | Connector, 1 Pin | Trompeter | J12-5 | 34-0400-0007 |
| P1 | Connector, 1 Pin | Amphenol | 27-26 | 34-0400-0004 |
| **CONNECTOR PLATE ASSEMBLY (BNC) - 02-2751-2263** | | | | |
| P1 | Connector, 1 Pin | Amphenol | 27-26 | 34-0400-0004 |
| **MECHANICAL ASSEMBLY - 02-2752-2110** | | | | |
| A12 | 5-7V Regulator Assembly | Bowmar/ALI | 02-2751-2290 | 02-2751-2290 |
| **FRONT PANEL ASSEMBLY - 02-2752-2122** | | | | |
| J28 | Connector, 3 Pin | Switchcraft | EAC-302 | 34-0300-0008 |
| S14 | Switch, Pushbutton | C & K | 8121YZE | 31-0017-0000 |
| S16 | Switch, SPDT | C & K | 5101ZQE | 31-0020-0000 |
| S18 | Switch, SPDT | C & K | 7101L2PY1ZQE | 31-0073-0000 |
| **MONITOR ASSEMBLY - 02-2753-2351** | | | | |
| A15 | DSX P.C. Board Assembly | Bowmar/ALI | 02-2753-2310 | 02-2753-2310 |
| J3-4 | Connector, 1 Pin | Trompeter | J3WE-5 | 34-0400-0005 |
| P1-2 | Connector, 1 Pin | Amphenol | 27-26 | 34-0400-0004 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **POWER CABLE ASSEMBLY - 02-2751-2160** | | | | |
| J20 | Connector, 2 Pin | AMP | 640250-2 | 34-0300-0009 |
| J19 | Connector, 3 Pin | AMP | 640250-3 | 34-0300-0006 |
| J29-30 | Terminal | Thomas & Betts | RA10 | 34-1400-0023 |
| P18,26 | Connector, 2 Pin | AMP | 1-350354-9 | 34-0300-0003 |
| P120 | Connector, 2 Pin | AMP | 1-480319-0 | 34-0300-0050 |
| P8 | Connector, 3 Pin | AMP | 640250-3 | 34-0300-0006 |
| P9 | Connector, 7 Pin | AMP | 640250-7 | 34-0300-0007 |
| P109 | Connector, 8 Pin | AMP | 1-480345-0 | 34-0300-0051 |
| **TIMEBASE CABLE ASSEMBLY - 02-2751-2170** | | | | |
| P1-2 | Connector, 34 Pin | Ansley | 609-3441 | 34-0200-0010 |
| **+5V POWER SUPPLY ASSEMBLY - 02-2751-2210** | | | | |
| C3 | Capacitor, 1.20µf, 25V, 10% | Sprague | 196D125X9025HA1 | 11-0400-0042 |
| C2 | Capacitor, 2.20µf, 25V, 10% | Sprague | 196D225X9025HA1 | 11-0400-0043 |
| CR1 | Diode, General Purpose | | 1N4148 | 20-0009-0000 |
| CR2-3 | Diode, Rectifier | | 1N4720 | 20-0012-0000 |
| J8 | Connector, 3 Pin | AMP | 640388-3 | 34-0300-0001 |
| Q2 | Integraged Circuit, VOLT-REG | Fairchild | UA78H05SC | 22-0008-0000 |
| Q1 | Transistor, Low Power, NPN | | 2N3904 | 21-0003-0000 |
| R9-10 | Resistor, 10.0K, 1% | | RLR07C1002F | 10-1501-1004 |
| R1-2,5 | Resistor, 12.1K, 1% | | RN55C1212F | 10-0201-1214 |
| R7 | Resistor, 2.74K, 1% | | RLR07C2741F | 10-1501-2743 |
| R4 | Resistor, 357 ohm, 1% | | RN55C3570F | 10-0201-3572 |
| R3 | Resistor, 37.4K, 1% | | RN55C3742F | 10-0201-3744 |
| R6 | Resistor, 51.1K, 1% | | RN55C5112F | 10-0201-5114 |
| R8 | Resistor, 90.9K, 1% | | RLR07C9092F | 10-1501-9094 |
| U1 | Integrated Circuit, Q-NET | RCA | CA3045 | 22-0004-0000 |
| U2 | Integrated Circuit, 2-NAND | Texas Inst. | SN7400N | 80-23-0200-0600 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **DMX MONITOR OPTION ASSEMBLY - 02-2753-2310** | | | | |
| C1,3,5,7 | Capacitor, .001µf, 50V, 20% | Unitrode | CGC102MDZ | 11-0600-0047 |
| C9-12,14-15 | Capacitor, 0.10µf, 50V, 80,-20% | Unitrode | CGD104ZDZ | 80-11-0600-0036 |
| C[illegible] | Capacitor, 0.33µf, 50V, 20% | Unitrode | CGF334MDZ | 11-0600-0048 |
| C2,4,6,8 | Capacitor, 1.00µf, 50V, 20% | Centralab | CY30C105M | 11-0600-0023 |
| J[illegible] | Connector, 14 Pin | Ansley | 609-1427 | 34-0200-0015 |
| J2-[illegible] | Connector, 1Pin | Amphenol | 27-800 | 34-0400-0003 |
| Q1-[illegible] | Transistor, Low Power NPN | | 2N2369A | 21-0001-0000 |
| R1[illegible] | Resistor, 500 ohm | Beckman | 89PR500 | 10-0100-0039 |
| R11,18,23 | Resistor, 1.00K, 1% | | RLR07C1001F | 10-1501-1003 |
| R9 | Resistor, 10 ohm, 1% | | RLR07C10R0F | 10-1501-1001 |
| R[illegible] | Resistor, 100 ohm, 1% | | RLR07C1000F | 10-1501-1002 |
| R2 | Resistor, 200 ohm, 1% | | RLR07C2000F | 10-1501-2002 |
| R5,19 | Resistor, 22.1 ohm, 1% | | RLR07C22R1F | 10-1501-2211 |
| R6 | Resistor, 274 ohm, 1% | | RLR07C2740F | 10-1501-2742 |
| R4-[illegible] | Resistor, 3.01K, 1% | | RLR07C3011F | 10-1501-3013 |
| R13 | Resistor, 39.2K, 1% | | RLR07C3922F | 10-1501-3924 |
| R16 | Resistor, 49.9 ohm, 1% | | RLR07C49R9F | 10-1501-4991 |
| R10 | Resistor, 511 ohm, 1% | | RLR07C5110F | 10-1501-5112 |
| R[illegible] | Resistor, 75 ohm, 1% | | RLR07C75R0F | 10-1501-7501 |
| R[illegible] | Resistor, 866 ohm, 1% | | RLR07C8660F | 10-1501-8662 |
| U[illegible] | Integrated Circuit, OP-AMP | Motorola | MC1590G | 22-0006-0000 |
| **LINEAR POWER SUPPLY ASSEMBLY - 02-2752-2550** | | | | |
| J25 | Connector, 6 Pin | AMP | 1-480340-0 | 34-0300-0082 |
| **TIMER CABLE ASSEMBLY - 02-2751-2130** | | | | |
| P5-6 | Connector, 26 Pin | Ansley | 609-2641 | 34-0200-0007 |
| **DISPLAY CABLE ASSEMBLY - 02-2751-2140** | | | | |
| P3-4 | Connector, 20 Pin | Ansley | 609-2041 | 34-0200-0005 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **NRZ OPTION 1 P.C. BOARD ASSEMBLY - 02-2753-2220 (Con't)** | | | | |
| R15-16 | Resistor, 365 ohm, 1% | | RLR07C3650F | 10-1501-3652 |
| R27-28 | Resistor, 43.2 ohm, 1% | | RN55C43R2F | 10-0201-4301 |
| R17-20 | Resistor, 475 ohm, 1% | | RLR07C4750F | 10-1501-4752 |
| R5-6 | Resistor, 499 ohm, 1% | | RLR07C4990F | 10-1501-4992 |
| R23-24 | Resistor, 51.1 ohm, 1% | | RLR07C51R1F | 10-1501-5111 |
| R21-22 | Resistor, 68.1 ohm, 1% | | RLR07C68R1F | 10-1501-6811 |
| R13-14 | Resistor, 750 ohm, 1% | | RLR07C7500F | 10-1501-7502 |
| U1-2 | Integrated Circuit LINE RCU | Fairchild | F10116PC | 80-23-1100-0018 |
| **NRZ OPTION 2 P.C. BOARD ASSEMBLY - 02-2753-2230** | | | | |
| C2 | Capacitor, 10.0µf, 20V, 10% | Sprague | 196D106X9020JA1 | 80-11-0400-0044 |
| C1 | Capacitor, 0.01µf, 50V, 80,-20% | Unitrode | CGC103ZDZ | 80-11-0600-0032 |
| P11 | Connector, 14 Pin | Ansley | 609-1407 | 34-0200-0011 |
| R5,7 | Resistor, 121 ohm, 1% | | RLR07C1210F | 10-1501-1212 |
| R2,10 | Resistor, 162 ohm, 1% | | RLR07C1620F | 10-1501-1622 |
| R4,6 | Resistor, 200 ohm, 1% | | RLR07C2000F | 10-1501-2002 |
| R1,9 | Resistor, 261 ohm, 1% | | RLR07C2610F | 10-1501-2612 |
| R3,8 | Resistor, 475 ohm, 1% | | RLR07C4750F | 10-1501-4752 |
| U2 | Integrated Circuit, 3/4 NOR | Fairchild | F10123PC | 23-1100-0019 |
| U1 | Integrated Circuit, LINE RCU | Fairchild | F10115PC | 80-23-1100-0017 |
| **5-7V REGULATOR ASSEMBLY - 02-2751-2290** | | | | |
| C4 | Capacitor, 1.20µf, 25V, 10% | Sprague | 196D125X9025HA1 | 11-0400-0042 |
| C2-3 | Capacitor, 2.20µf, 25V, 10% | Sprague | 196D225X9025HA1 | 11-0400-0043 |
| C1 | Capacitor, 600µf, 25V | Sprague | 500D607G025FK5 | 11-0500-0064 |
| CR1-2 | Diode | | 1N4001 | 20-0000-0000 |
| J120 | Connector, 2 Pin | AMP | 1-480318-0 | 34-0300-0049 |
| P19 | Connector, 3 Pin | AMP | 640388-3 | 34-0300-0001 |
| R1 | Resistor, 100 ohm | Beckman | 89PR100 | 10-0100-0037 |
| R2 | Resistor, 301 ohm, 1% | | RLR07C3010F | 10-1501-3012 |
| VR1 | Integrated Circuit, VOLT-REG | National | LM320MLP-5.0 | 22-0003-0000 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **DISPLAY MODULE ASSEMBLY - 02-2752-2510 (Cont.)** | | | | |
| U1-2 | Integrated Circuit, DSPL-BUF | Intersil | ICM7212AMIPL | 23-0006-0000 |
| U3-5 | Integrated Circuit, D-FLOP | Texas Inst. | SN7474N | 80-23-0200-0620 |
| U6-7 | Integrated Circuit, ENCODER | Texas Inst. | SN74147N | 80-23-0200-0637 |
| U8 | Integrated Cicuit, INVERTER | Texas Inst. | SN7404N | 80-23-0200-0603 |
| XDS16-21 | Connector, 14 Pin | Circuit Assy. | CA14S-10SD | 34-1300-0002 |
| XU1 | Connector, 40 Pin | Augat | 540-AG10D | 34-1300-0014 |
| **POWER SUPPLY ASSEMBLY - 02-2751-2180** | | | | |
| A9 | Power Supply Assembly | Bowmar/ALI | 02-2751-2210 | 02-2751-2210 |
| A13 | Power Supply | Power General | 1050-1A | 62-0100-0001 |
| C1 | Capacitor, 31K, 15V | Mepco-Eelctra | 3120EC313U015AM | 11-0500-0065 |
| J18 | Connector, 2 Pin | AMP | 1-350351-9 | 34-0300-0005 |
| **NRZ OPTION 1 P.C. BOARD ASSEMBLY - 02-2753-2220** | | | | |
| C14-15 | Capacitor, 10.0µf, 20V, 10% | Sprague | 196D106X9020JA1 | 80-11-0400-0044 |
| C5-12 | Capacitor, 0.01µf, 50V, 80,-20% | Unitrode | CGC103ZDZ | 80-11-0600-0032 |
| C1-4 | Capacitor, 0.10µf, 50V, -20/80% | AVX | MA205E104Z | 11-0600-0046 |
| J11 | Connector, 14 Pin | Ansley | 609-1407 | 34-0200-0011 |
| Q1-6 | Transistor, Low Power, NPN | | 2N2369A | 21-0001-0000 |
| Q7-8 | Transistor, Low Power, PNP | | 2N4209 | 21-0007-0000 |
| R31-34 | Ressitor, 500 ohm, 15T | Beckman | 89WR500 | 10-0100-0058 |
| R29-30 | Resistor, 107 ohm, 1% | | RN55C1070F | 10-0201-1072 |
| R9-10 | Resistor, 15 ohm, 1% | | RLR07C15R0F | 10-1501-1501 |
| R25-26 | Resistor, 150 ohm, 1% | | RN55C1500F | 10-0201-1502 |
| R3-4 | Resistor, 162 ohm, 1% | | RLR07C1620F | 10-1501-1622 |
| R1-2 | Resistor, 261 ohm, 1% | | RLR07C2610F | 10-1501-2612 |
| R7-8 | Resistor, 301 ohm, 1% | | RLR07C3010F | 10-1501-3012 |
| R11-12 | Resistor, 36.5 ohm, 1% | | [illegible] | 10-1501-3651 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **TIMER MODULE ASSEMBLY - 02-2752-2520** | | | | |
| C1 | Capacitor, 10.0µf, 20V, 10% | Sprague | 196D106X9020JA1 | 80-11-0400-0044 |
| C2 | Capacitor, 0.10µf, 50V, 20% | Unitrode | CTC104MDZ | 80-11-0600-0038 |
| E1-3 | Terminal | Cambion | 160-2027-02-01-00 | 34-1400-0002 |
| J5 | Connector, 26 Pin | Ansley | 609-2607ES | 34-0200-0006 |
| R2-20 | Resistor, 1.00K, 1% | | RLR07C1001F | 10-1501-1003 |
| S17 | Switch | C & K | 312610B4101069 | 31-0021-0000 |
| S15 | Switch | C & K | 332610B01 | 31-0022-0000 |
| U1 | Integrated Circuit, I/O EXPO | Intel | P8243 | 24-0000-0005 |
| **DISPLAY MODULE ASSEMBLY - 02-2752-2510** | | | | |
| C1,3 | Capacitor, 10.0µf, 20V, 10% | Sprague | 196D106X9020JA1 | 80-11-0400-0044 |
| C2 | Capacitor, 0.01µf, 50V, 80,-20% | Unitrode | CGC103ZDZ | 80-11-0600-0032 |
| CR1-5 | Diode, General Purpose | | 1N4148 | 20-0009-0000 |
| DS16-21 | Display, LED, 7-Segment | Hewlett Packard | 5082-7650 | 14-0002-0000 |
| DS2 | Display, LED, Green | Hewlett Packard | HLMP-3502 | 14-0046-0000 |
| DS3,4,6,8,10, DS12,14,15 | Display, LED, Red | Hewlett Packard | HLMP-3300 | 14-0003-0000 |
| DS1,5,7,9,11,13 | Display, LED, Yellow | Hewlett Packard | HLMP-3400 | 14-0025-0000 |
| J3 | Connector, 20 Pin | Ansley | 609-2007 | 34-0200-0003 |
| J1 | Connector, 34 Pin | Ansley | 609-3407 | 34-0200-0009 |
| R21,37-46,48-56 | Resistor, 1.00K, 1% | | RLR07C1001F | 10-1501-1003 |
| R13 | Resistor, 10.0K, 1% | | RLR07C1002F | 10-1501-1004 |
| R22-36 | Resistor, 274 ohm, 1% | | RLR07C2740F | 10-1501-2742 |
| S1-2 | Switch, Rotary | Grayhill | 24878-10N | 31-0023-0000 |
| S7 | Switch, DPDT | C & K | 7203L2PY9V30QE | 31-0014-0000 |
| S3-5, 10 | Switch, SPDT | C & K | 7101L2PY9V30QE | 31-0011-0000 |
| S6,8-9 | Switch, SPDT | C & K | 7103L2PY9V30QE | 31-0013-0000 |
| S13 | Switch, SPDT | C & K | 7105L2PY9V30QE | 31-0015-0000 |
| S11-12 | Switch, SPDT | C & K | P8121V30E | 31-0016-0000 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **TIMEBASE MODULE ASSEMBLY - 02-2752-2500 (Con't)** | | | | |
| U30 | Integrated Circuit, 8BIT CPU | Intel | P8035HL | 24-0000-0001 |
| U11,15 | Integrated Circuit, I/O EXPO | Intel | P8243 | 24-0000-0005 |
| U19,28 | Integrated Circuit, I/O PORT | Intel | P8212 | 24-0000-0002 |
| U14,17,23 | Integrated Circuit, TIMER | Intel | P8254 | 24-0000-0004 |
| U29 | Integrated Circuit, USART | Intel | P8251A | 24-0000-0003 |
| U13,20 | Integrated Circuit, 2-NAND | Texas Inst. | SN7400N | 80-23-0200-0600 |
| U25 | Integrated Circuit, 4-16 DCDR | Texas Inst. | SN74154N | 23-0200-0641 |
| U12 | Integrated Circuit, 8D-LATCH | Texas Inst. | SN74LS373N | 23-0300-0662 |
| U16,22,26 | Integrated Circuit, INVERTER | Texas Inst. | SN7404N | 80-23-0200-0603 |
| U18 | Integrated Circuit, ONE SHOT | Texas Inst. | SN7123N | 80-23-0200-0636 |
| XU31 | Connector, 24 Pin | Augat | 524-AG10D | 34-1300-0013 |
| XU30 | Connector, 40 Pin | Augat | 540-AG10D | 34-1300-0014 |
| Y1 | Crystal, 6.00 MHz | Valpey-Fisher | VF600 | 15-0300-0003 |
| **INTERCONNECT BOARD ASSEMBLY - 02-2752-2540** | | | | |
| E1-10 | Terminal | Cambion | 160-2027-02-01-00 | 34-1400-0002 |
| J26 | Connector, 2 Pin | AMP | 1-350351-9 | 34-0300-0005 |
| J109 | Connector, 8 Pin | AMP | 1-480283-0 | 34-0300-0052 |
| P12-17 | Connector, 100 Pin | AMP | 2-530841-2 | 34-0100-0001 |
| P10 | Connector, 14 Pin | Ansley | 609-1427ES | 34-0200-0002 |
| P4 | Connector, 20 Pin | Ansley | 609-2027 | 34-0200-0004 |
| P6 | Connector, 26 Pin | Ansley | 609-2607ES | 34-0200-0006 |
| P2 | Connector, 34 Pin | Ansley | 609-3407ES | 34-0200-0008 |
| P20 | Connector, 2 Pin | AMP | 640388-2 | 34-0300-0004 |
| P25 | Connector, 6 Pin | AMP | 1-480270-0 | 34-0300-0081 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **TIMEBASE MODULE ASSEMBLY - 02-2752-2500** | | | | |
| C1,3,21,25 | Capacitor, 0.10µf, 35V, 10% | Sprague | 196D104X9035HA1 | 11-0400-0096 |
| C2,14,20.24 | Capacitor, 10.0µf, 20V, 10% | Sprague | 196D106X9020JA1 | 80-11-0400-0044 |
| C17 | Capacitor, 47.0µf, 20V, 10% | Sprague | 196D476X9020PE4 | 80-11-0400-0097 |
| C4-7,10-13, C18,19,22,23, C26-34 | Capacitor, 0.01µf, 50V, 80,-20% | Unitrode | CGC103ZDZ | 80-11-0600-0032 |
| C16 | Capacitor, 20.0pf, 500V, 5% | | CM04ED200J03 | 11-0300-0042 |
| C8,9 | Capacitor, 300 pf, 300V, 2% | | CM04FC301G03 | 11-0300-0024 |
| C15 | Capacitor, 5.00pf, 500V, 5% | | CM04CD050D03 | 11-0300-0006 |
| CR1-2 | Diode, General Purpose | | 1N4148 | 20-0009-0000 |
| E1-4 | Terminal | Cambion | 160-2027-02-01-00 | 34-1400-0002 |
| L1-4 | Ferrite Bead | Ferronics | 21-031-B | 15-1100-0000 |
| P24 | Connector, 25 Pin D-Type | AMP | 205857-2 | 34-0300-0076 |
| R21,33-37,41,42 | Resistor, 1.00K, 1% | | RLR07C1001F | 10-1501-1003 |
| R1,7,26,28,30-31 | Resistor, 160 ohm, 5% | | RLR07C1600J | 10-1301-1602 |
| R38,39 | Resistor, 20.0K, 5% | | RLR07C2002J | 10-1301-2004 |
| R2,8,25,27,29,32 | Resistor, 270 ohm, 5% | | RLR07C2700J | 10-1301-2702 |
| R10,15 | Resistor, 5.10K, 5% | | RLR07C5101J | 10-1301-5103 |
| R3-6,9,11-14,16, R17-20,22-24 | Resistor, 470 ohm, 5% | | RLR07C4700J | 10-1301-4702 |
| S19-20 | Switch, DPDT | Alco Elec. | MSS-2250R | 31-0072-0000 |
| U31 | Integrated Circuit, EPROM | Intel | D2732A-4 | 24-0000-0006 |
| U32 | Integrated Circuit, DRIVER | National | DS1488N | 23-0004-0000 |
| U21 | Integrated Circuit, RECEIVER | National | DS1489AN | 23-0005-0000 |
| U1,6 | Integrated Circuit, BCD CNTR | Fairchild | F10010PC | 80-23-1100-0002 |
| U4,5 | Integrated Circuit, D-FLOP | Fairchild | F10231PC | 80-23-1100-0047 |
| U2-3,7-8 | Integrated Circuit, ECL-TTL | Fairchild | F10125PC | 80-23-1100-0021 |
| U10 | Integrated Circuit, EX-NOROR | Fairchild | F10107PC | 80-23-1100-0011 |
| U9 | Integrated Circuit, TTL-ECL | Fairchild | F10124PC | 80-23-1100-0020 |
| U24,27 | Integrated Circuit, 4-BIT, BUS DRIVER | Intel | P8216 | 24-0000-0007 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **SYNC MODULE ASSEMBLY - 02-2752-2530 (Cont.)** | | | | |
| R23,39,40<br>R42-47,52,53,55 | Resistor, 1.00K, 1% | | RLR07C1001F | 10-1501-1003 |
| R2,4,5,8,10,12,<br>R15,19,21,28,30,<br>R31,36,37,56 | Resistor, 162 ohm, 1% | | RLR07C1620F | 10-1501-1622 |
| R33,48,50,51,54 | Resistor, 20.0K, 1% | | RN55C2002F | 10-0201-2004 |
| R1,3,6,9,11,13,<br>R14,20,22,27,29,<br>R32,35,38,57 | Resistor, 261 ohm, 1% | | RLR07C2610F | 10-1501-2612 |
| R34 | Registor, 29.4K, 1% | | RN55C2942F | 10-0201-2944 |
| R7 | Resistor, 475 ohm, 1% | | RLR07C4750F | 10-1501-4752 |
| R16 | Resistor, 5.11K, 1% | | RLR07C5111F | 10-1501-5113 |
| R24 | Resistor, 511 ohm, 1% | | RLR07C5110F | 10-1501-5112 |
| R41,49 | Resistor, 7.8K, 1% | | RN55C7871F | 10-0201-7873 |
| RN6-9,12,13<br>R15-18,21-22 | Resistor Network | CTS | 750-81-R470 | 22-0000-0000 |
| U6 | Integrated Circuit, 2NOR | Fairchild | F10102PC | 80-23-1100-0006 |
| U12 | Integrated Circuit, OR | Fairchild | F10103PC | 80-23-1100-0007 |
| U2-5,9,13,15 | Integrated Circuit, BIN CNTR | Fairchild | F10016PC | 80-23-1100-0003 |
| U1,8,16,17 | Integrated Circuit, D-FLOP | Fairchild | F10131PC | 80-23-1100-0023 |
| U18-19 | Integrated Circuit, ECL-TTL | Fairchild | F10125PC | 80-23-1100-0021 |
| U7 | Integrated Circuit, EX-NOROR | Fairchild | F10107PC | 80-23-1100-0011 |
| U26,31,34 | Integrated Circuit, 2-NAND | Texas Inst. | SN7400N | 80-23-0200-0600 |
| U23,30,32 | Integrated Circuit, 3-NAND | Texas Inst. | SN7410N | 80-23-0200-0605 |
| U21-22 | Integrated Curcuit, D-FLOP | Texas Inst. | SN7474N | 80-23-0200-0620 |
| U35 | Integrated Curcuit, DEC CNTR | Texas Inst. | SN7490AN | 80-23-0200-0626 |
| U20,24,25,33 | Integrated Circuit, ONE SHOT | Texas Inst. | SN74123N | 80-23-0200-0636 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **FRAME & DATA MODULE ASSEMBLY - 02-2751-2030 (Con't)** | | | | |
| RN2-13,15-16, RN19-20,22-27, RN29-30 | Resistor Network | CTS | 750-81-R470 | 22-0000-0000 |
| U1,5,10,11,19 | Integrated Circuit, 2 NOR | Fairchild | F10102PC | 80-23-1100-0006 |
| U20 | Integrated Circuit, OR | Fairchild | F10103PC | 80-23-1100-0007 |
| U9 | Integrated Circuit, 2/3 NOR | Fairchild | F10106PC | 80-23-1100-0010 |
| U6 | Integrated Circuit 4LN MUX | Fairchild | F10174PC | 80-23-1100-0037 |
| U3,4,8,21 | Integrated Circuit, 6D-FLOP | Fairchild | F10176PC | 80-23-1100-0039 |
| U2,16,18 | Integrated Circuit, BIN CNTR | Fairchild | F10016PC | 80-23-1100-0003 |
| U12,14-15,24 | Integrated Circuit, D-FLOP | Fairchild | F10131PC | 80-23-1100-0023 |
| U23 | Integrated Circuit, ECL-TTL | Fairchild | F10125PC | 80-23-1100-0021 |
| U7, 13 | Integrated Circuit, EC-NOROR | Fairchild | F10107PC | 80-23-1100-0011 |
| U22, 25 | Integrated Cirucit, TTL-ECL | Fairchild | F10124PC | 80-23-1100-0020 |
| U27, 33 | Integrated Circuit, 2-NAND | Texas Inst. | SN7400N | 80-23-0200-0600 |
| U26, 28 | Integrated Circuit, 3-NAND | Texas Inst. | SN7410N | 80-23-0200-0605 |
| U30, 32 | Integrated Circuit, BCD-DEC | Texas Inst. | SN7442AN | 80-23-0200-0611 |
| U29,31,35 | Integrated Circuit, BIN CNTR | Texas Inst. | SN74161N | 80-23-0200-0648 |
| U34 | Integrated Circuit, D-FLOP | Texas Inst. | SN7474N | 80-23-0200-0620 |
| **SYNC MODULE ASSEMBLY - 02-2752-2530** | | | | |
| C1, 24 | Capacitor, 10.0µf, 20V, 10% | Sprague | 196D106X9020JA1 | 80-11-0400-0044 |
| C10,12,17,19,22 | Capacitor, 33.0µf, 6V, 10% | Sprague | 196D336X9006JA1 | 11-0400-0045 |
| C13,16 | Capacitor, .010µf, 250V | Siemens | B32540C-.01-5-250 | 11-1100-0017 |
| C2-9,14,15,18, C20,21,23 | Capacitor, 0.01µf, 50V, 80,-20% | Unitrode | CGC103ZDZ | 80-11-0600-0032 |
| C11 | Capacitor, 270pf, 500V, 5% | | CM05FD271J03 | 11-0300-0064 |
| CR1,4-9 | Diode, General Purpose | | 1N4148 | 20-0009-0000 |
| L1-2 | Ferrite Bead | Ferronics | 21-031-B | 15-1100-0000 |
| Q1 | Transistor, Low Power, NPN | | 2N3904 | 21-0003-0000 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **CODE MODULE ASSEMBLY- 02-2751-2020 (Con't)** | | | | |
| S1 | Switch, SPDT, Pushbutton | C & K | 8121DZE | 31-0018-0000 |
| U2,4,5,9,17,19 | Integrated Circuit, 2 NOR | Fairchild | F10102PC | 80-23-1100-0006 |
| U1,11,13 | Integrated Circuit, 2 OR | Fairchild | F10103PC | 80-23-1100-0007 |
| U23 | Integrated Circuit, 2/3 NOR | Fairchild | F10106PC | 80-23-1100-0010 |
| U10,20 | Integrated Circuit, 3/4 NOR | Fairchild | F10123PC | 23-1100-0019 |
| U24 | Integrated Circuit, 4/5 NOROR | Fairchild | F10109PC | 80-23-1100-0012 |
| U3 | Integrated Circuit, 4 LN MUX | Fairchild | F10174PC | 80-23-1100-0037 |
| U7,12,25 | Integrated Circuit, 6D-FLOP | Fairchild | F10176PC | 80-23-1100-0039 |
| U6,14,22 | Integrated Circuit, D-FLOP | Fairchild | F10231PC | 80-23-1100-0047 |
| U15 | Integrated Circuit, ECL-TTL | Fairchild | F10125PC | 80-23-1100-0021 |
| U18 | Integrated Circuit, EX-NOROR | Fairchild | F10107PC | 80-23-1100-0011 |
| U8 | Integrated Circuit, JK-FLOP | Fairchild | F10135PC | 80-23-1100-0026 |
| U16 | Integrated Circuit, TTL-ECL | Fairchild | F10124PC | 80-23-1100-0020 |
| U27 | Integrated Circuit, 1-8 MUX | Texas Inst. | SN74151AN | 80-23-0200-0639 |
| U26 | Integrated Circuit, 3-NAND | Texas Inst. | SN7410N | 80-23-0200-0605 |
| U28-35 | Integrated Circuit, DEC Counter | Texas Inst. | SN7490AN | 80-23-0200-0626 |
| U21 | Integrated Circuit, Inverter | Texas Inst. | SN7404N | 80-23-0200-0603 |
| **FRAME & DATA MODULE ASSEMBLY - 02-2751-2030** | | | | |
| C1,12 | Capacitor, 10.0µf, 20V, 10% | Sprague | 196D106X9020JA1 | 80-11-0400-0044 |
| C2-9,11,13-15 | Capacitor, 0.01µf, 50V, 80,-20% | Unitrode | CGC103ZDZ | 80-11-0600-0032 |
| CR1,3,4 | Diode, General Purpose | | 1N4148 | 20-0009-0000 |
| L1, 2 | Ferrite Bead | Ferronics | 21-031-B | 15-1100-0000 |
| R23-28,32 | Resistor, 1.00K, 1% | | RLR07C1001F | 10-1501-1003 |
| R3,6,7,9, R12-13,18-19, R22, 34 | Resistor, 162 ohm, 1% | | RLR07C1620F | 10-1501-1622 |
| R2,4,5,8,11,14, R16,17,21,33 | Resistor, 261 ohm, 1% | | RLR07C2610F | 10-1501-2612 |
| R1,15,20,30-31 | Resistor, 5.11K, 1% | | RLR07C5111F | 10-1501-5113 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **INTERFACE MODULE ASSEMBLY - 02-2751-2012 (Con't)** | | | | |
| U2,3,5,7 | Integrated Circuit, Line RCU | Fairchild | F10116PC | 80-23-1100-0018 |
| U1,13,20 | Integrated Circuit, Op-Amp | Fairchild | UA747PC | 22-0007-0000 |
| Y1 | Crystal, 44.736 MHz | Int. Crystal | 471540 | 15-0300-0004 |
| **CODE MOUDLE ASSEMBLY - 02-2751-2020** | | | | |
| C1,17-19 | Capacitor, 10.0µf, 20V, 10% | Sprague | 196D106X9020JA1 | 80-11-0400-0044 |
| C2-16,20 | Capacitor, 0.01µf, 50V, 80,-20% | Unitrode | CGC103ZDZ | 80-11-0600-0032 |
| CR2-3 | Diode, General Purpose | | 1N4148 | 20-0009-0000 |
| J 3-7 | Connector, Single, 1 Pin | Trompeter | BJ27 | 34-0400-0002 |
| L1-2 | Ferrite Bead | Ferronics | 21-031-B | 15-1100-0000 |
| R30, 31, 43 | Resistor, 1.00K, 1% | | RLR07C1001F | 10-1501-1003 |
| R27, 28 | Resistor, 100 ohm, 1% | | RLR07C1000F | 10-1501-1002 |
| R18 | Resistor, 130 ohm, 1% | | RLR07C1300F | 10-1501-1302 |
| R4,6,8,10,12,14, R16,20,22,24,34, R36,38,40,42,44, R46,49 | Resistor, 162 ohm, 1% | | RLR07C1620F | 10-1501-1622 |
| R19 | Resistor, 200 ohm,1% | | RLR07C200F | 10-1501-2002 |
| R3,5,7,11,13,15, R17,21,23,25,33, R35,37,39,41,45, R47,48 | Resistor, 261 ohm, 1% | | RLR07C2610F | 10-1501-2612 |
| R2,9,26,29 | Resistor, 5.11K, 1% | | RLR07C5111F | 10-1501-5113 |
| RN2,4-13,16-19, RN21,23-25, RN27,28,30 | Resistor Network | CTS | 750-81-R470 | 22-0000-0000 |
| S1 | Switch, Type 1 | C & K | 8018 | 31-0028-0000 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **INTERFACE MODULE ASSEMBLY - 02-2751-2012 (Con't)** | | | | |
| R51 | Resistor, 3.92K, 1% | | RLR07C3921F | 10-1501-3923 |
| R150 | Resistor, 39.2K, 1% | | RLR07C3922F | 10-1501-3924 |
| R19 | Resistor, 4.42K, 1% | | RN55C4421F | 10-0201-4423 |
| R85,112 | Resistor, 432 ohm, 1% | | RLR07C4320F | 10-1501-4322 |
| R25 | Resistor, 442 ohm, 1% | | RN55C4420F | 10-0201-4422 |
| R18,36-38,41,42, R46,48,53,55, R96-99,123-126, R147 | Resistor, 475 ohm, 1% | | RLR07C4750F | 10-1501-4752 |
| R35,40 | Resistor, 49.9 ohm, 1% | | RLR07C49R9F | 10-1501-4991 |
| R105,146 | Resistor, 49.9K, 1% | | RN55C4992F | 10-0201-4994 |
| R29,32 | Resistor, 51.1 ohm, 1% | | RN55C51R1F | 10-0201-5111 |
| R65,68,71,74,77, R109 | Resistor, 51.1 ohm, 1% | | RLR07C51R1F | 10-1501-5111 |
| R45 | Resistor, 511 ohm, 1% | | RLR07C5110F | 10-1501-5112 |
| R84,113 | Resistor, 562 ohm, 1% | | RLR07C5620F | 10-1501-5622 |
| R61 | Resistor, 6.98K, 1% | | RLR07C6981F | 10-1501-6983 |
| R1,3,6,8,9,15, R90-91,94,95,102, R103,111,116,119, R121,122,129,143 | Resistor, 75 ohm, 1% | | RN55C75R0F | 10-0201-7501 |
| R57 | Resistor, 750 ohm, 1% | | RN55C7500F | 10-0201-7502 |
| R100,127 | Resistor, Select, 1% | | RLR07 Type | 02-2751-5012 |
| R101,128 | Resistor, Select, 1% | | RLR07 Type | 02-2751-5011 |
| RN8-10,14-17, RN21-24 | Resistor Network | CTS | 750-81-R470 | 22-0000-0000 |
| T1,2 | Transformer, RF, Z=50 | Mini-Circuits | T1-1T | 13-0006-0000 |
| U11,18 | Integrated Circuit, Q-NET | RCA | CA3054 | 22-0005-0000 |
| U4,6,15 | Integrated Circuit, NOR | Fairchild | F10102PC | 80-23-1100-0006 |
| U10,14 | Integrated Circuit, OR | Fairchild | F10103PC | 80-23-1100-0007 |
| U12,19 | Integrated Circuit, 4-Bit NOR/OR | Fairchild | F10109PC | 80-23-1100-0012 |
| U16,17,21-24 | Integrated Circuit, MD-FLOP | Fairchild | F10176PC | 80-23-1100-0039 |
| U8,9 | Integrated Circuit, Binary Counter | Fairchild | F10016PC | 80-23-1100-0003 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **INTERFACE MODULE ASSEMBLY - 02-2751-2012 (Con't)** | | | | |
| R56 | Resistor, 1.00K, 15T | Beckman | 89PR1K | 10-0100-0040 |
| R16,30,31 | Resistor, 1.00K, 1% | | RN55C1001F | 10-0201-1003 |
| R43,59,62, R131,133 | Resistor, 1.00K, 1% | | RLR07C1001F | 10-1501-1003 |
| R28 | Resistor, 1.27K, 1% | | RN55C1271F | 10-0201-1273 |
| R58 | Resistor, 1.82K, 1% | | RN55C1821F | 10-0201-1823 |
| R11,17,33, R60,144 | Resistor, 10.0 ohm, 1% | | RLR07C10R0F | 10-1501-1001 |
| R83 | Resistor, 10.0 ohm, 1% | | RLR32C10R0F | 10-1503-1001 |
| R21,34,39 | Resistor, 100 ohm, 1% | | RLR07C1000F | 10-1501-1002 |
| R22,104,142 | Resistor, 100K, 1% | | RN55C1003F | 10-0201-1005 |
| R7, 10 | Resistor, 12.7 ohm, 1% | | RN55D12R7F | 10-0208-1271 |
| R64,67,70,73, R76,88,108 | Resistor, 121 ohm, 1% | | RLR07C1210F | 10-1501-1212 |
| R79,81,110 | Resistor, 130 ohm, 1% | | RLR07C1300F | 10-1501-1302 |
| R5 | Resistor, 14.7 ohm, 1% | | RN55D14R7F | 10-0208-1471 |
| R92,115,118 | Resistor, 147 ohm, 1% | | RN55C1470F | 10-0201-1472 |
| R137,139,140,149 | Resistor, 162 ohm, 1% | | RLR07C1620F | 10-1501-1622 |
| R2,93,117 | Resistor, 17.8 ohm, 1% | | RN55D17R8F | 10-0208-1781 |
| R20,24,27 | Resistor, 2.21K, 1% | | RN55C2211F | 10-0201-2213 |
| R66,69,72,75,78, R80,82,86,107, R114 | Resistor, 20.0 ohm, 1% | | RLR07C20R0F | 10-1501-2001 |
| R12-14 | Resistor, 200 ohm, 1% | | RLR07C2000F | 10-1501-2002 |
| R49,54 | Resistor, 22.1 ohm, 1% | | RLR07C22R1F | 10-1501-2211 |
| R44 | Resistor, 22.1K, 1% | | RLR07C2212F | 10-1501-2214 |
| R50, 52 | Resistor, 243 ohm, 1% | | RLR07C2430F | 10-1501-2432 |
| R134-136,141,148 | Resistor, 261 ohm, 1% | | RLR07C2610F | 10-1501-2612 |
| R4,89,120 | Resistor, 274 ohm, 1% | | RN55C2740F | 10-0201-2742 |
| R130,132 | Resistor, 3.01K, 1% | | RLR07C3011F | 10-1501-3013 |
| R23, 26 | Resistor, 3.24K, 1% | | RN55C3241F | 10-0201-3243 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **INTERFACE MODULE ASSEMBLY - 02-2751-2012** | | | | |
| C1,50,65,73 | Capacitor, 10.0µf, 20V, 10% | Sprague | 196D106X9020JA1 | 80-11-0400-0044 |
| C22,23,26 | Capacitor, 1-20pf | Johanson Mfg. | 5501 | 11-0100-0001 |
| C4-12,14-20,24, C28-30,32-33,39, C43-49,53,54,57, C60,61,63,64, C66-71,74-79 | Capacitor, 0.01µf, 50V, 80,-20% | Unitrode | CGC103ZDZ | 80-11-0600-0032 |
| C34-38,40,41, C56,59 | Capacitor, 0.10µf, 50V, 20% | Unitrode | CGC104MDZ | 80-11-0600-0038 |
| C13,42,62 | Capacitor, 100pf, 500V | | CM04FD101G03 | 80-11-0300-0051 |
| C21 | Capacitor, 2.00pf, 500V | | CM04CD020D03 | 11-0300-0063 |
| C2 | Capacitor, 22.0pf, 500V, 5% | | CM04ED220J03 | 80-11-0300-0038 |
| C27 | Capacitor, 30.0pf, 500V, 5% | | CM04CD300J03 | 80-11-0300-0057 |
| C25 | Capacitor, 5.00pf, 500V, 5% | | CM04CD050D03 | 80-11-0300-0006 |
| C3, 31 | Capacitor, 2200pf, 50V, 10% | AVX Corp. | MA105C222K | 11-0600-0044 |
| C100-101 | Capacitor, Select, 5% | | CM04 Type | 02-2751-5010 |
| CR1-4 | Diode, General Purpose | | 1N4148 | 20-0009-0000 |
| J1 | Connector, Single, 1 Pin | Amphenol | 27-800 | 34-0400-0003 |
| K1-3 | Mounting Pad | Thermalloy | 7717-30 | 61-0700-0002 |
| K1-3 | Relay, Radio Frequency, 5VDC | HI-G | CAW-5 | 30-0008-0000 |
| L2 | Inductor, 0.22µh, 10% | Lenox-Fugle | NR-.22 | 12-0016-0000 |
| L3-6, 8 | Inductor, 0.56µh, 10% | Lenox-Fugle | NR-.56 | 12-0015-0000 |
| L1,7,9-11 | Ferrite Bead | Ferronics | 21-031-B | 15-1100-0000 |
| Q10-18 | Mounting Pad | Thermalloy | 7717-178 | 61-0700-0003 |
| Q10-18 | Transistor, Low Power, NPN | | 2N3866 | 21-0030-0000 |
| Q1-9 | Transistor, Low Power, NPN | | 2N2369A | 21-0001-0000 |
| Q19-20 | Transistor, Low Power, NPN | | 2N3904 | 21-0003-0000 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | MANUFACTURER'S PART NUMBER | BOWMAR/ALI'S PART NUMBER |
|---|---|---|---|---|
| **MAIN ASSEMBLY (02-2752-2000)** | | | | |
| A1 | Interface Module Assembly | Bowmar/ALI | 02-2751-2012 | 02-2751-2012 |
| A2 | Code Module Assembly | Bowmar/ALI | 02-2751-2020 | 02-2751-2020 |
| A3 | F & D Module Assembly | Bowmar/ALI | 02-2751-2030 | 02-2751-2030 |
| A4 | Sync Module Assembly | Bowmar/ALI | 02-2752-2530 | 02-2752-2530 |
| A5 | Timebase Module Assembly | Bowmar/ALI | 02-2752-2500 | 02-2752-2500 |
| A6 | Interconnect Module Assembly | Bowmar/ALI | 02-2752-2540 | 02-2752-2540 |
| A7 | Timer Module Assembly | Bowmar/ALI | 02-2752-2520 | 02-2752-2520 |
| A8 | Display Module assembly | Bowmar/ALI | 02-2752-2510 | 02-2752-2510 |

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